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FB-2502 CPU Card
Half Size Pentium User's Manual

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If you have problems or difficulties in using the system board, or setting up the relevant devices, and software that are not explained in this manual, please contact our service engineer for service, or send email to support@fabiatech.com.

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If your board requires servicing, contact the dealer from whom you purchased the product for service information. You can help assure efficient servicing of your product by following these guidelines:

- A list of your name, address, telephone, facsimile number, or email address where you may be reached during the day
- Description of you peripheral attachments
- Description of you software (operating system, version, application software, etc.) and BIOS configuration
- Description of the symptoms (Extract wording any message)

For updated BIOS, drivers, manuals, or product information, please visit us at www.fabiatech.com

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Chapter 1 Introducing the FB-2502 System Board

Overview

The FB-2502 is a Pentium all–in-one CPU card. This user's manual provides information on the physical features, installation, and BIOS setup of the FB2502.

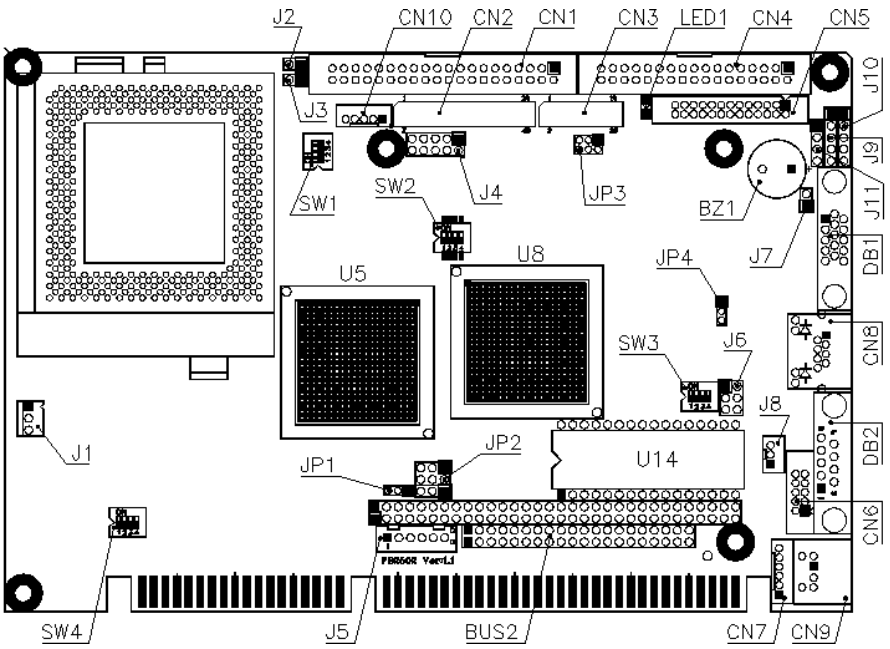
Built to unleash the total potential of the Pentium Processor, the FB2502 is a single boards computer capable of handling today's demanding requirements. Able to support low power Tillamook and Pentium MMX CPUs, this unit supports 10/100M MII interface network port, synchronous pipe line burst SDRAM on board 32MB up to 64MB, External cache 512KB, DiskOnChip (DOC) or 512k SRAM, and a 2MB PCI -VGA controller that can support LCD's and CRT's simultaneously or independently.

Each FB2502 has two ports for I/O communications. One RS-232C and one RS-232C /485 ports are available. There is also a watchdog timer that can be configured from software to automatically reset the system or generate an interrupt if there is a system's or EMI problem. And for easy configuration, AMI BIOS are available.

Power management is also featured to lower the rate of consumption. The unit supports doze mode, <Suspend Mode> and <Standby mode> as well as it adheres to the "Green Function" standard.

The FB2502 is perfect for POS and POI applications, network systems, panel / MMI's, order entry kiosks, test equipment, OEM projects or as a motherboard for a panel PC. The unit is only 185X122mm, offering unparalleled performance in a very small footprint.

Layout


J2
CN10
CN2
CN1
CN3
LED1
CN4
CN5
J10
J3
J9
J11
SW1
SW2
J4
JP3
BZ1
J7
DB1
U8
JP4
U5
SW3
J6
CN8
J8
J1
JP2
U14
DB2
JP1
CN6
SW4
J5
BUS2
CN7
CN9

Specifications

- Supports all dual power socket-7 CPUs with 66.7Mhz front side bus (FSB)
- Compact size slot card with ISA PC/104 expansion bus.
- Intel 440TX chipset and 512KB L2 cache.
- Supports on-board 32MB SDRAM, 64MB maximum.
- 100M/10M Ethernet with RJ-45 connector.
- C&T 69000 chipset provides CRT and LCD interface with 2MB VRAM.
- Parallel port, floppy and PCI IDE Interface.
- 1 RS-232C and 1 RS-232C/RS-422/RS-485/IrDA.
- PS/2 compatible keyboard and mouse interface.
- E2KEY function for safe CMOS data keeping. (Optional item)
- On-board buzzer and LED indicator.
- Flash BIOS with easy upgrade utility.
- Software programmable watchdog timer.
- Provides 1 socket for up to 288MB DiskOnChip or up to 512k SRAM.
- 2 USB ports and Provides CPU cooling fan connector.
- Provide 2 SMD type SRAM space for up to 1.5MB SRAM disk (Optional item)
- EMI Considered on every output signals.
- Power Req.: +5v 2.5A maximum and +12V 30mA maximum (based on 266MHz Low Power CPU)
- Compact size, 185 mm x 122 mm.

Packing List

Upon receiving the package, verify the following things. Should any of the mentioned happens, contact us for immediate service.

- Unpack and inspect the FB2502 package for possible damage that may occur during the delivery process.
- Verify the accessories in the package according to the packing list and see if there is anything missing or incorrect package is included.
- If the cable(s) you use to install the FB2502 is not supplied from us, please make sure the specification of the cable(s) is compatible with the FB2502 system board.

Note: after you install the FB2502, it is recommended that you keep the diskette or CD that contains drivers and document files, document copies, and unused cables in the cartoon for future use.

The following lists the accessories that may be included in your FB2502 package. Some accessories are optional items that are only shipped upon order.

- One FB2502 all-in-one CPU board
- One compact disc containing manual file in PDF format and necessary drivers and utilities
- One 40-pin hard disk drive interface cable
- One 34-pin floppy drive interface cable
- One serial port and parallel port interface cable with bracket
- One 2-port USB adapter cable (Optional)

Chapter 2 Hardware Installation

To set up a FB2502 system board, complete the description n Chapter 2 and Chapter 3.

This chapter introduces the system board connectors, jumper settings and then guides you to apply them for field application.

Before Installation

Before you install the system board, make sure you follow the following descriptions.

1. Before removing the board from its anti-static bag, wear an anti-static strap to prevent the generation of Electricity Static Discharge (ESD). The ESD may be created from human body that touches the board. It may do damage to the board circuit.

2. Install or unplug any connector, module, or add-on card, be sure that the power is disconnected from the system board. If not, this may damage the system board components, module, or the add-on-card.

3. Installing a heat sink and cooling fan is necessary for heat dissipation from your CPU. If heat sink or cooling fan is not mounted, this may cause the CPU fail due to over-heating problem.

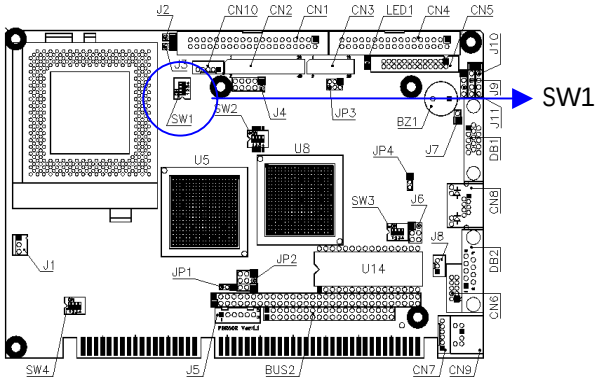
4. When you connect the connectors and memory modules, be careful with the pin orientations.

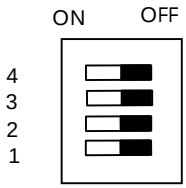
Hardware Features

The following lists the connectors and jumpers to install the FB2502.

Item	Description
CN1	40-pin 2.54mm IDE hard disk connector
CN2, CN3	DF12 40/20 –PIN LCD interface connector
CN4	34-pin 2.54mm floppy connector
CN5	26-pin 2.0 mm parallel port connector
CN6	10-pin 2.0 mm RS-232 connector
CN7, CN9	Keyboard and Mouse connector
CN8	RJ45-Lan connector
CN10	5-pin external header for inverter board
J1	3-pin for CPU cooling fan
J2	2-pin HDD LED Indicator
J3	2-pin Reset header
J4	USB connector
J5	6 –pin power connector
J6	6-pin for 2 In /Out TTL bits
J7	2-pin external battery header
J8	3-pin RS232C touch screen header for serial port 2
J9	5-pin keyboard lock and external LED header
J10	5-pin for external Infra module
J11	4-pin for external speaker Connector
JP1	Select 5V or 3.3V for SRAM.
JP2	Select DOC or SRAM
JP3	Select LVDS or Panel Link signal
JP4	3-pin Select internal or external battery
DB1	CRT connector
DB2	9-pin D – type male connector
LED1	Power and watchdog of LED indicator
SW1	To select internal clock multiplier and external base clock
SW2	To select the type of LCD panel
SW3	To select RS232/RS422 and RS485 select for serial port 2
SW4	To select V-Core and V-IO Voltage

SW1 (1,2,3,4): Selecting CPU Internal Clock Multiplier



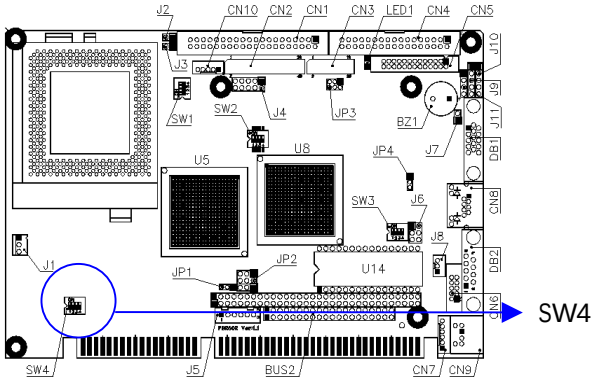


The following lists the switch settings of CPU Internal Clock Multiplier.

SW1-1	SW1-2	SW1-3	SW1-4	Internal Clock Multiplier			Remark
				INTEL (P55C)	Tillamook (P55C)	AMD K6	
Off	Off	Off	Off	-	-	3.5	
On	Off	Off	Off	-	-	2.0	
Off	On	Off	Off	-	-	3.0	
On	On	Off	Off	-	4.0	2.5	Default
Off	Off	On	Off	3.5	-	3.5	
On	Off	On	Off	2.0	-	2.0	
Off	On	On	Off	3.0	-	3.0	
On	On	On	Off	2.5	2.5	2.5	
Off	Off	Off	On	-	-	5.5	
On	Off	Off	On	-	-	4.0	
Off	On	Off	On	-	-	5.0	
On	On	Off	On	-	4.0	4.5	
Off	Off	On	On	3.5	-	5.5	
On	Off	On	On	2.0	-	4.0	
Off	On	On	On	3.0	-	5.0	
On	On	On	On	2.5	2.5	4.5	

Note: The CPUs must setup their clock multiplier internally, so it is necessary to set SW1 any more.

SW4 (1,2,3,4): Selecting CPU V-IO & VCORE Voltage



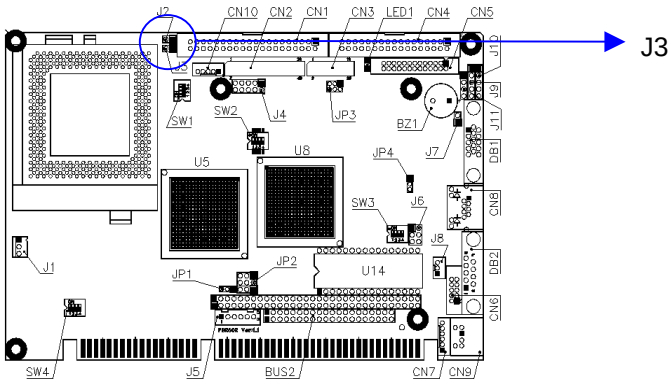
The following lists the switch settings of CPU V-CORE & VIO voltage.

SW4-1	SW4-2	SW4-3	V-Core	Remark
Off	On	On	1.9V	Default
On	On	On	2.0V	
On	Off	Off	2.3V	
Off	Off	On	2.8V	
Off	Off	On	3.1V	
Others is reserved				

SW4-4	V-IO	Remark
Off	3.3V	
On	2.5V	Default for Tillamook CPU only

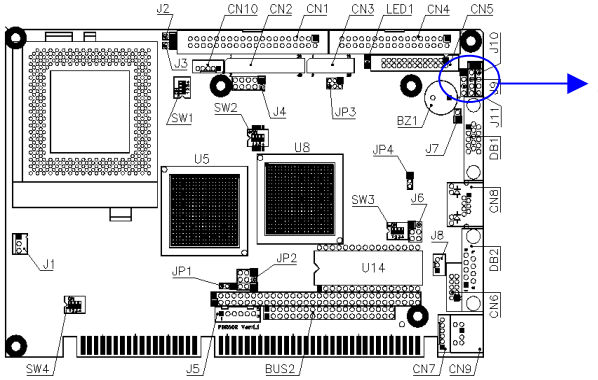
J3: Reset Header

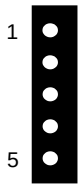
J3 is a 2-pin header for connecting to system reset bottom. Short-circuit these 2 pins to hardware reset FB2502 as well as restart system. It is similar to power off the system and then power it on again.



1.Reset +
2.Reset -

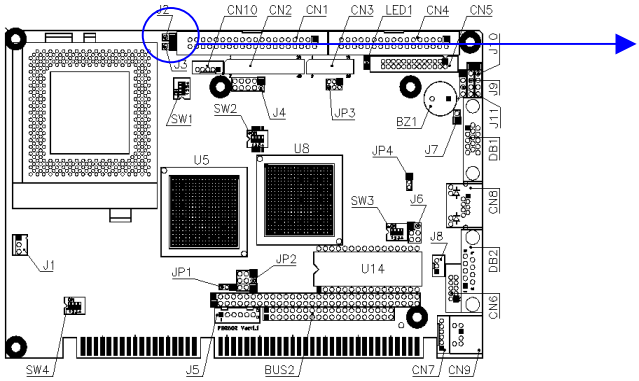
J9: Power LED Header

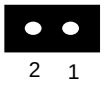




Pin 1: Power LED +
Pin 2: N.C
Pin 3: Power LED -
Pin 4: Keyboard Lock
Pin 5: Ground

J2: HDD LED Header

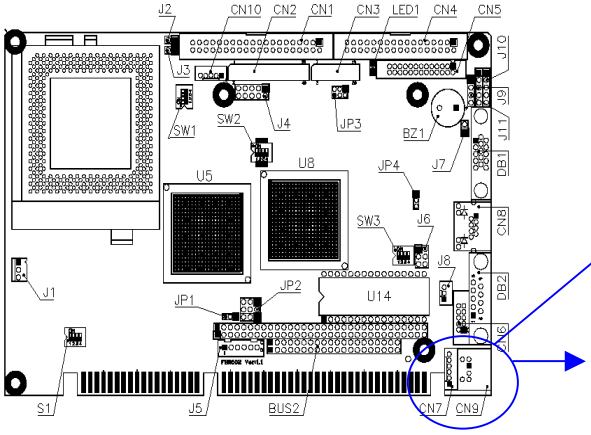


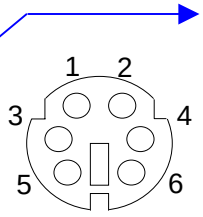


1.Hard Disk LED+
2.Hard Disk LED -

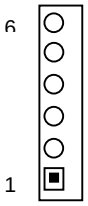
CN7, CN9: Keyboard/Mouse Connector

CN9 is a standard PS/2 type keyboard connector, so any PS/2 type keyboard can plug into CN9 directly without extra adapter cable. CN9 provides PS/2 mouse interface, use the included mouse adapter cable to connect between CN7 and standard PS/2 mouse.





CN9 Front View

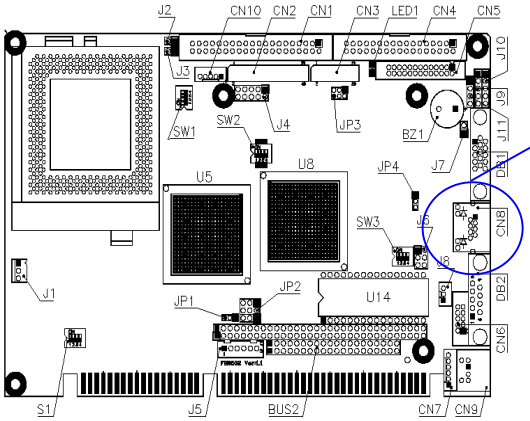


CN7

CN7	CN9	Signal
1	2	Mouse Data
2	1	Keyboard Data
3	3	Ground
4	4	VCC
5	6	Mouse Clock
6	5	Keyboard Clock

CN8: RJ45 LAN Connector

The CN8 contain LAN twist pair signals and LAN accesses indicator signal is RJ45 type connector with 2 LED indicators. The down side LED (orange) indicates data is accessing and the up side LED (green) indicates on-line status. (When lighted indicates on-line and off indicates off-line).



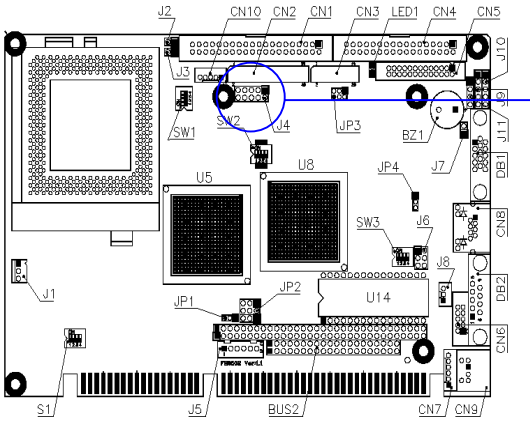
CN8

The following lists the pin assignment of RJ45.

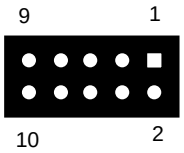
RJ45	Signal	RJ45	Signal
1	TPTX+	5	FBG1
2	TPTX -	6	TPRX -
3	TPRX+	7	FBG2
4	FBG1	8	FBG2

J4: USB Connector

J4 is a 10-pin connector. Use included adapter cable (Optional) for transfering to standard double port USB connector. The upper port is USB #1 and the lower port is USB#2



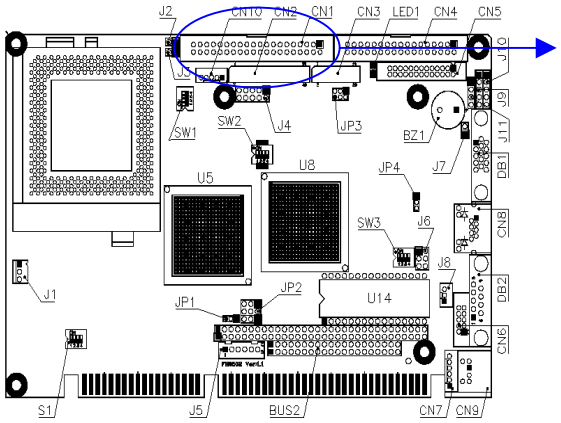
J4

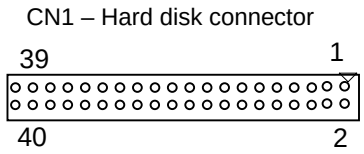


J4	Signal	J4	Signal
1	USBV0	2	Case Ground
3	USBD0+	4	USBG1
5	USBD0-	6	USBD1-
7	USBG0	8	USBD1+
9	Case Ground	10	USBV1

CN1: IDE hard Disk Connector

CN 1 is 40-pin 2.54mm IDE hard disk connector. The included hard disk cable is able to attach up to two 3.5" hard disk drives.



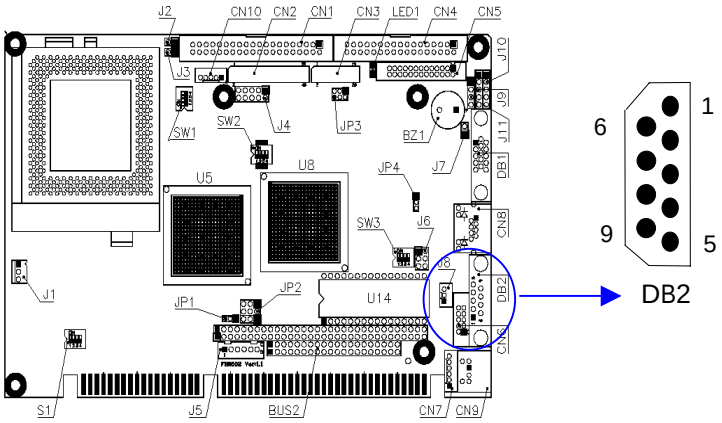


The following table lists the pin description of CN1.

Pin	Signal	Pin	Signal
1	-RESET	2	GROUND
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	GROUND	20	NOT USED
21	IDEDREQ	22	GROUND
23	-IOW A	24	GROUND
25	-IOR A	26	GROUND
27	IDEIORDYA	28	GROUND
29	-DACKA	30	GROUND
31	AINT	32	GROUND
33	SA 1	34	Not Used
35	SA 0	36	SA 2
37	CS 0	38	CS 1
39	HD LED A	40	GROUND

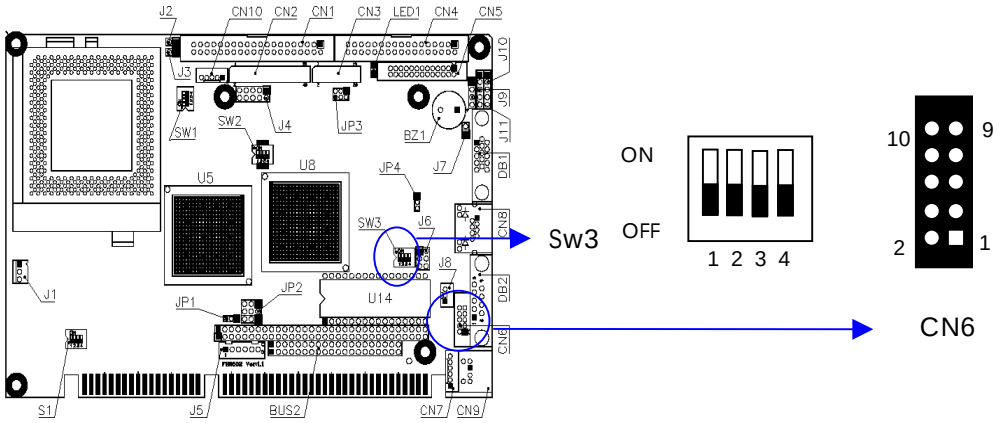
DB2: RS232 Serial Ports 1 Connectors and Jumpers

The DB2 connector on bracket is 9-pin D-type male connector the serial port 2 adapter cables are used to transfer 10-pin IDC connector into standard DB9 connectors.



Serial Port 2 (CN6, SW3, J8 and J10)

Serial port 2 is designed for multiple proposes. It could be RS-232C or RS-422 or RS-485 by selecting SW3, and SW3-4 is use to enable or disable terminator if RS422 or RS-485 mode is selected. Serial port 2 also could be configured as Infra (IrDA) interface by changing the setting in BIOS setup program. J10 is use to interface with Infra module. When touch screen module is used, you could connect J8 to touch screen controller directly and internally instead of connect from CN6 connector.



The following tables and figures show the pin definitions usage:

SW3-1	SW3-2	Mode Of Port 2	Remark
Off	Off	RS-232C	Default
On	Off	RS-485	
On	On	RS-422	

The following tables and figures show the Terminator usage:

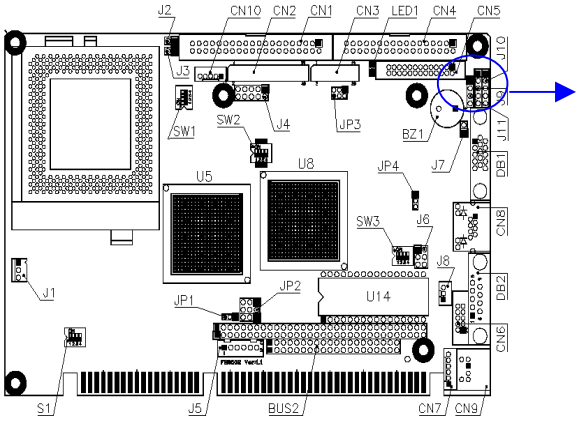
SW3-4	Terminator Resistor	Remark
Off	Disable	Default
On	Enable	

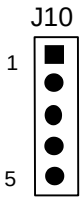
The Tables include serial port cable is use to transfer CN6 into standard 9-pin D-type male connector.

CN6	RS232C	RS-422	RS-485	DB9
1	-DCD2	-	-	1
2	-DSR2	-	-	6
3	RXD2	RXD-	485-	2
4	-RTS2	TXD-	-	7
5	TXD2	RXD+	485+	3
6	-CTS2	TX+	-	8
7	-DTR2	-	-	4
8	-RI2	-	-	9
9	GROUND2	GROUND2	GROUND2	5
10	CASE GROUND	CASE GROUND	CASE GROUND	-

J10: 5-pin Infrared Header

J10 provides infrared signals of serial port 2. The infrared signal is used to interface with Infrared modules.

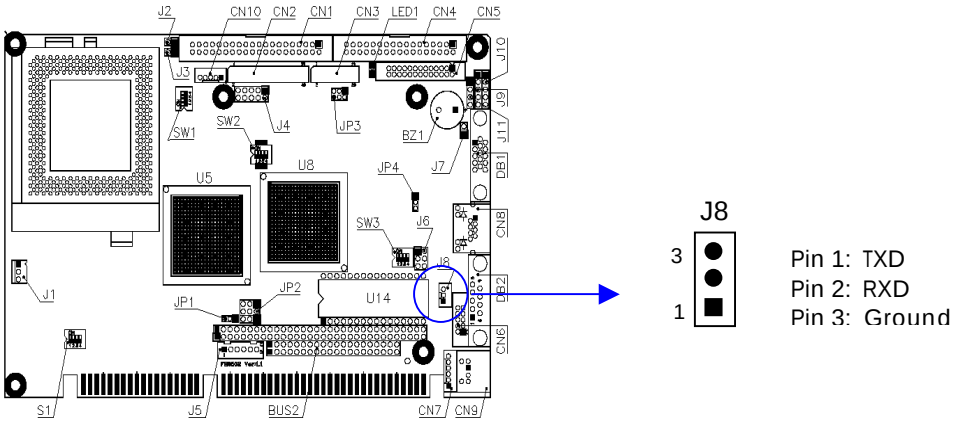




Pin 1: VCC
Pin 2: N.C.
Pin 3: IRRX
Pin 4: Ground
Pin 5: IRTX

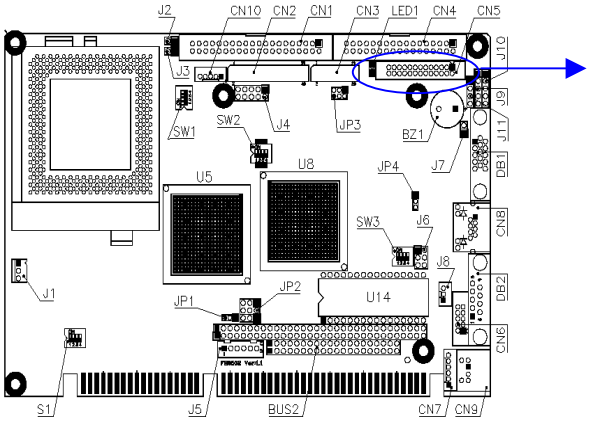
J8: Touch Screen Header

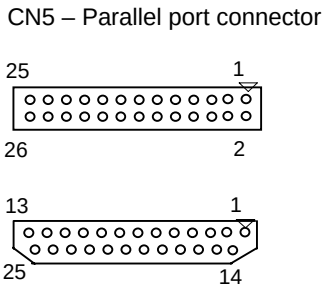
J8 provide basic RS-232C signals of serial port 2 respectively. The basic RS-232C signal is used to interface with touch screen controller internally.



CN5: 26-pin Parallel Port Connector

The included printer interface cable is used to transfer 26-pin connector into standard DB25 connector.

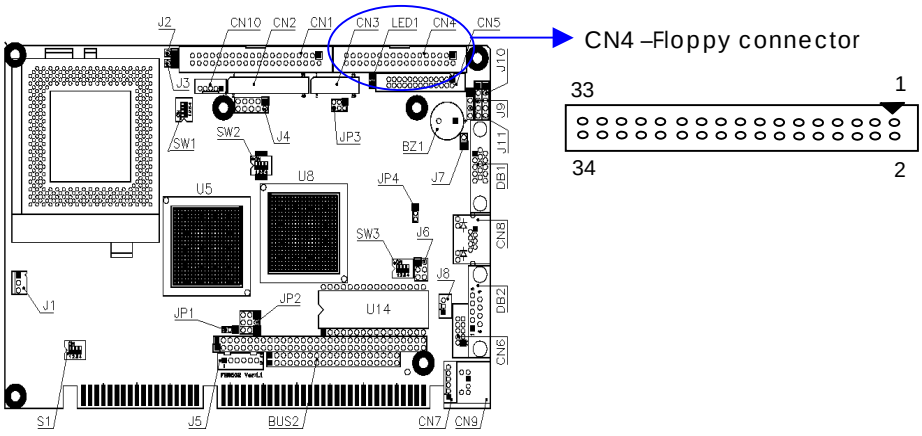




CN5	DB-25	Signal	CN5	DB-25	Signal
1	1	-STROBE	2	14	-AUTO FORM FEED
3	2	DATA 0	4	15	-ERROR
5	3	DATA 1	6	16	-INITIALIZE
7	4	DATA 2	8	17	-PRINTER SELECT IN
9	5	DATA 3	10	18	Ground
11	6	DATA 4	12	19	Ground
13	7	DATA 5	14	20	Ground
15	8	DATA 6	16	21	Ground
17	9	DATA 7	18	22	Ground
19	10	-ACKNOWLEDGE	20	23	Ground
21	11	BUSY	22	24	Ground
23	12	PAPER	24	25	Ground
25	13	PRINTER SELECT	26	--	No Used

CN4: Floppy Connector

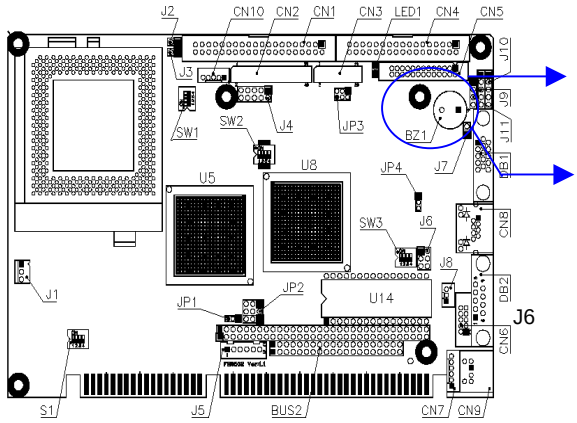
The included floppy drive interface cable is used standard 34-pin connector. The following table shows signal connections 34-pin connectors.



34-pin	Signal	34-pin	Signal
2	Drive Enable A	23	Ground
8	-Index	24	-Write Enable
12	-Select A	26	-Track 0
11	Ground	28	-Write Protect
16	-Motor A	29	Ground
14	- Select B	30	-Read Data
10	-Motor B	31	Ground
9	Ground	32	-Head
18	-Direction	33	NC
20	-Step	34	-Disk Change
22	-Write Data	Others	No Connection

BZ1: On-Board Buzzer (BZ1) & J11: External Speaker Header

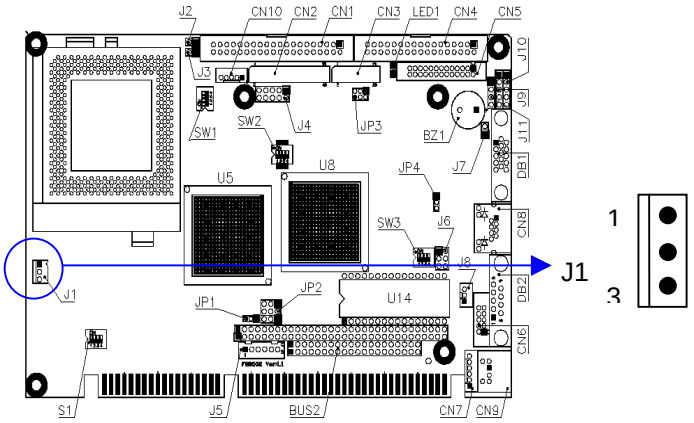
BZ1 is the on-board buzzer and you can use 2-pin or 4-pin cable connectors between and extra 8 ohms speaker with J11 header.



PIN	Signal
1	Speaker+
2	Speaker-
3	Speaker-
4	Speaker-

J1: CPU Fan Connector

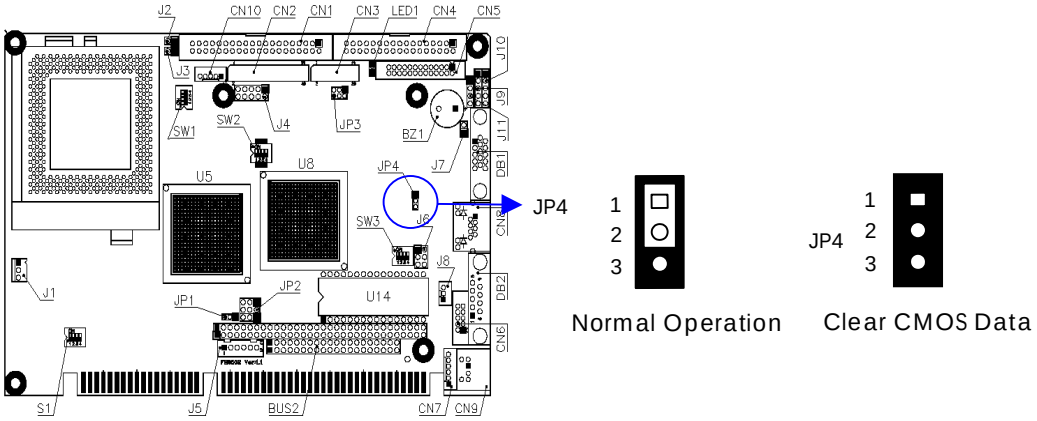
J1 is 3 pins Molex connector, which is used to driver CPU cooling fan if Non-Low-Power CPUs are used.



J1	Description
1	Ground
2	+12V
3	NC.

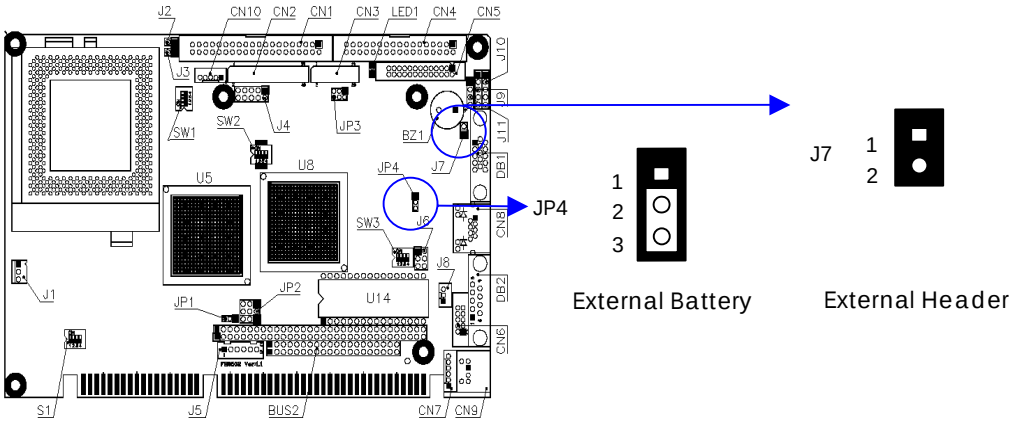
JP4: CMOS Data Clear Jumper

You can use JP4 to clear CMOS data. The CMOS store information like system date, time, boot up device, password, IRQ... that are set up with the BIOS. To clear the CMOS, set JP4 to open and then return to 1-2. The default setting is 1-2.



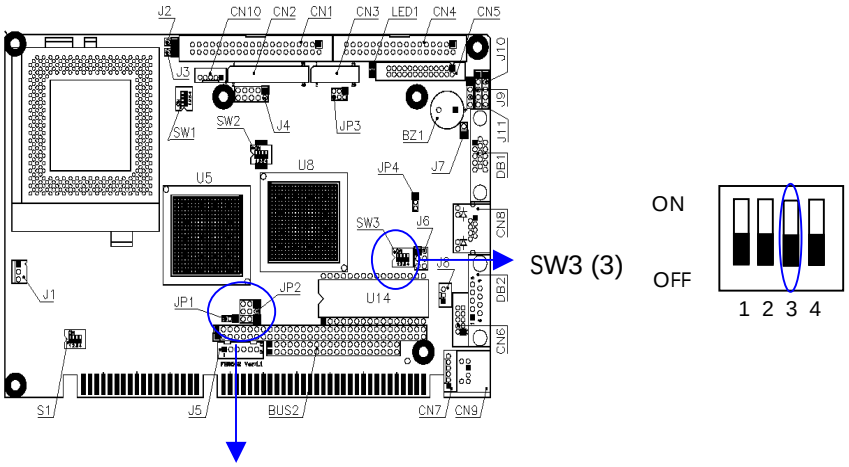
J7: External Battery Header

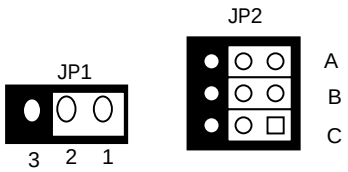
An external battery pack J7 that could be connected ensures data retention of SRAM; you can use J7 external battery to backup SRAM data.



SW3 (3): DiskOnChip Address Select

If DiskOnChip is to be used, select a mapping memory address for it. Two addresses are provided, CC00, D800. The default setting is CC00.



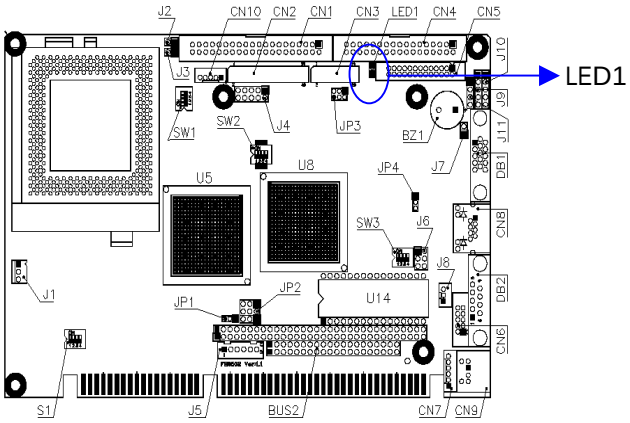


DiskOnChip
Factory Preset

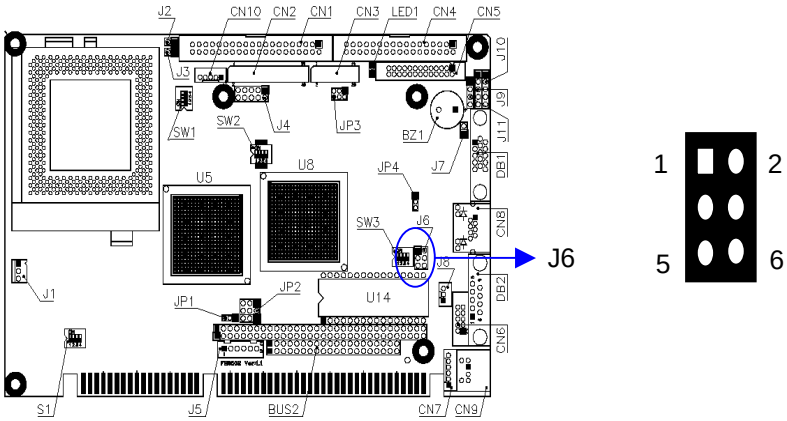
SW3-3	Mapping Segment	Remark
Off	CC00:0	Default
On	D800:0	

On-Board Power and Watchdog LED (LED1)

LED1 indicates power is active when it lights. If the watchdog is enabled, LED1 will blink in a stable period.

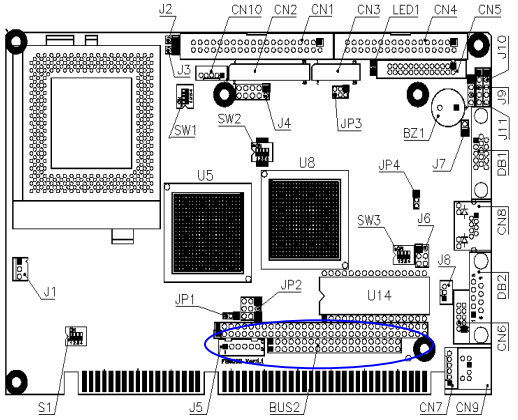


J6: TTL I/O Connector



J6	Signal	Bit Location	CN11	Signal	Bit Location
1	Input 0	Bit 3 Of Port 390H	2	Output 0	Bit 0 Of Port 390H
3	Input 1	Bit 2 Of Port 390H	4	Output 1	Bit 1 Of Port 390H
5	+5v	-	6	Ground	-

BUS2: PC/104 Connector



PC/104 A&B Pin

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	-IOCHK	A17	SA14	B1	Ground	B17	-DACK1
A2	SD7	A18	SA13	B2	RSTDRV	B18	DRQ1
A3	SD6	A19	SA12	B3	+5V	B19	-REFSH
A4	SD5	A20	SA11	B4	IRQ9	B20	BUSCLK
A5	SD4	A21	SA10	B5	-5V (*1)	B21	IRQ7
A6	SD3	A22	SA9	B6	DRQ2	B22	IRQ6
A7	SD2	A23	SA8	B7	-12V (*1)	B23	IRQ5
A8	SD1	A24	SA7	B8	-ZWS	B24	IRQ4
A9	SD0	A25	SA6	B9	+12V	B25	IRQ3
A10	IORDY	A26	SA5	B10	Key1	B26	-DACK2
A11	AEN	A27	SA4	B11	-MEMW	B27	TC
A12	SA19	A28	SA3	B12	-MEMR	B28	ALE
A13	SA18	A29	SA2	B13	-IOW	B29	+5V
A14	SA17	A30	SA1	B14	-IOR	B30	OSC
A15	SA16	A31	SA0	B15	-DACK3	B31	Ground
A16	SA15	A32	Ground	B16	DRQ3	B32	Ground

PC/104 C& D Pin

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
C1	GND	C11	MEMW#	D1	Ground	D11	-DACK#5
C2	SBHE	C12	SD8	D2	MEMCS16#	D12	DREQ5
C3	LA23	C13	SD9	D3	IOCS16#	D13	DACK#6
C4	LA22	C24	SD10	D4	IRQ10	D14	DREQ6
C5	LA21	C25	SD11	D5	IRQ11	D15	DACK#7
C6	LA20	C26	SD12	D6	IRQ12	D16	DREQ7
C7	LA19	C27	SD13	D7	IRQ15	D17	VCC
C8	LA18	C28	SD14	D8	IRQ14	D18	MASTER#
C9	LA17	C29	SD15	D9	DACK#0	D19	GND
C10	MEMR#	C20	KEY	D10	DREQ0	D20	GND

Chapter 3 Installing CRT and LCD Monitors

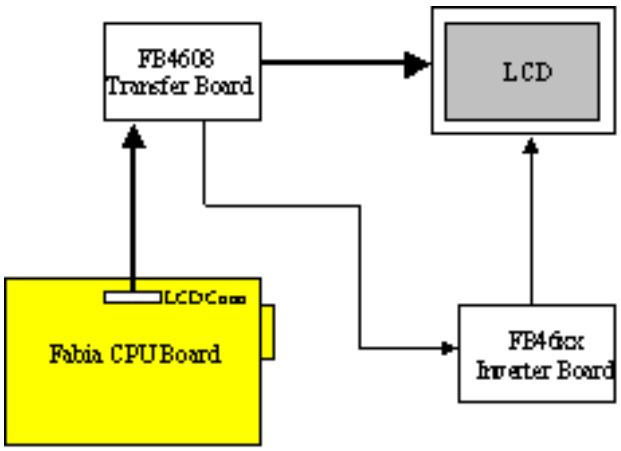
This chapter describes the configuration and installation procedure of LCD and CRT displays. Both CRT and LCD displays may be used at the same time. However, each type of LCD requires different BIOS. This section describes the configuration and installation procedure using LCD display. Skip this section if you are using CRT monitor only.

- LCD Flat Panel Display
- CRT & LCD Display

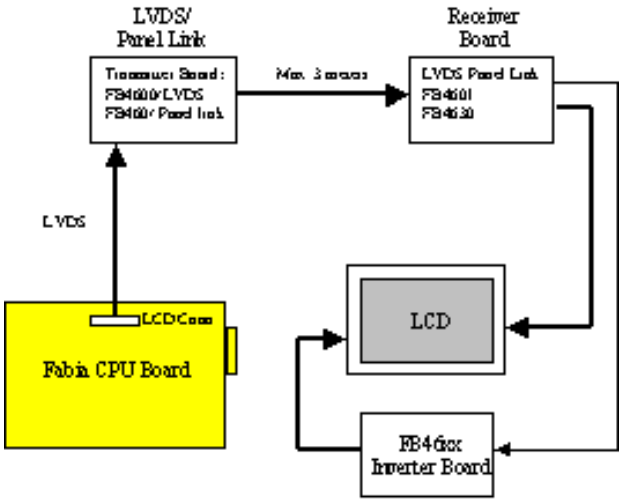
LCD FLAT PANEL DISPLAY

Using the SW2 configure the BIOS default setting for different types of LCD panel. And then set your system properly and configure BIOS module for the right type of LCD panel you are using. Each model of LCD requires different BIOS in order to work properly. If the BIOS you need is not on our website www.fabiatech.com, then you can send us a sample of the panel you will be using and we will send it back to you with the new BIOS.

The following shows the block diagram of using FB2502 for LCD display.



LCD Panel Block Diagram



LVDS/Panel Link Diagram

The block diagram shows that FB2502 till needs components to be used with a LCD panel. The transfer board (FB4608) provides the control for the brightness and the contrast of the LCD panel while inverter board (FB46xx) is the one that supplies the high voltage to drive the LCD panel. Both FB4608 and FB46xx are available from FabIATech with all the necessary cables.

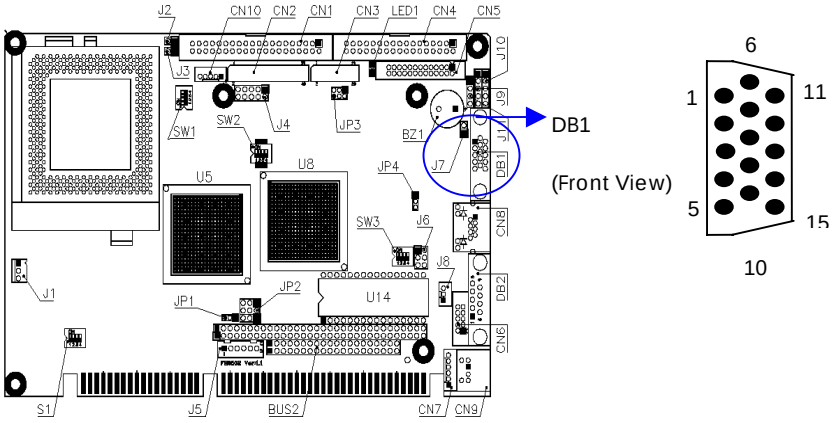
NOTE: Be careful with the pin orientation when installing connectors and the cables. A wrong connection can easily destroy your LCD panel. The pin 1 of the cable connectors is indicated with a sticker and the pin1 of the ribbon cable usually has a different color.

CRT & LCD DISPLAY

The FB2502 supports a CRT colored monitor and a LCD. It can be connected to create a compact video solution for the industrial environment. 2MB of RAM on-boarded allows a maximum CRT resolution of 1024X768 with 64K colors and a LCD resolution of 1024X768 with 64K colors.

DB1: CRT connector

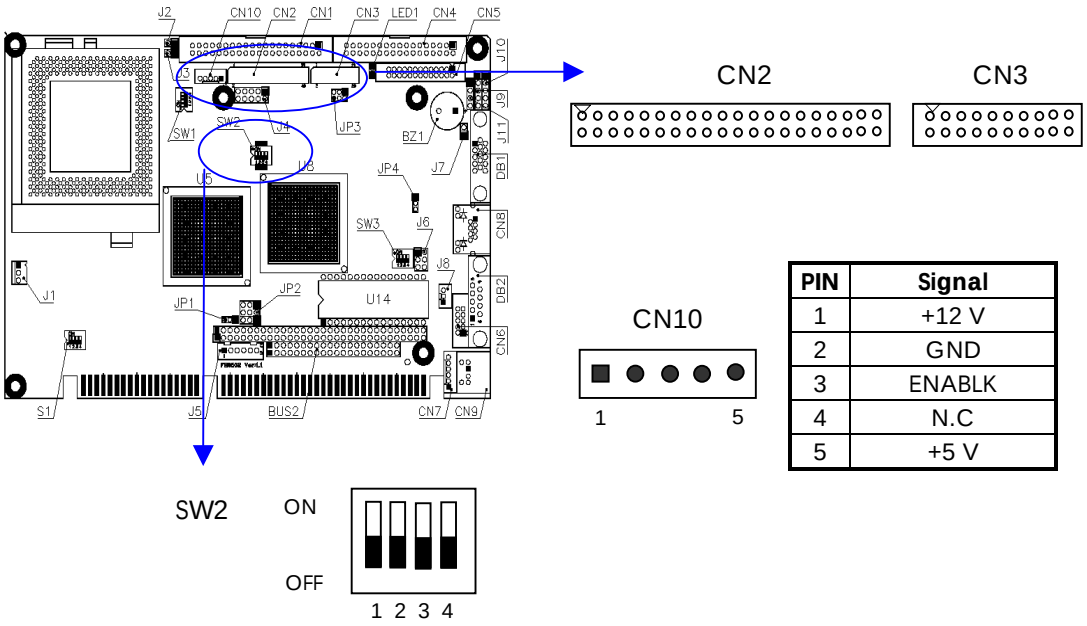
The CRT is use to a standard CRT connector (DB1).



DB15	Signal	DB15	Signal
1	RED	Case	Case Ground
2	GREEN	5,10	Digital Ground
3	BLUE	6,7,8	Analog Ground
14	VSYNC	15	DDC Clock
13	HSYNC	12	DDC Data

CN2, CN3: LCD Connector and Panel Type: SW2

CN2 and CN3 is 36-bit LCD interface connector and CN10 is inverter board connector. If LCD BIOS supported, SW2 is used to select which LCD panel type is used.



PIN	Signal
1	+12 V
2	GND
3	ENABLK
4	N.C
5	+5 V

Pin	CN2	CN3	Pin	CN2	CN3
1	+5V (*2)	Ground	2	+5V (*2)	Ground
3	Ground	FP24	4	Ground	FP25
5	+3.3V(*2)	FP26	6	+3.3V(*2)	FP27
7	NC (*2)	FP28	8	Ground	FP29
9	FP0	FP30	10	FP1	FP31
11	FP2	FP28	12	FP3	FP33
13	FP4	FP30	14	FP5	FP35
15	FP6	Ground	16	FP7	Ground
17	FP8	VB0 (1*)	18	FP9	VB1 (1*)
19	FP10	VB2 (1*)	20	FP11	VB3 (1*)
21	FP12		22	FP13	
23	FP14		24	FP15	
25	FP16 (SCK)		26	FP17	
27	FP18		28	FP19	
29	FP20		30	FP21	
31	FP22		32	FP23	
33	Ground		34	Ground	
35	SHFCLK		36	FP	
37	DE		38	LP	
39	ENABLK		40	ENAVEE	

Note 1: Signals from VB0 to VB3 pins are 3.3V level digital outputs. They could be used as LCD back light or GPIO controls.

Selecting LCD Panel: SW2

Item	SW2				LCD Panel Specification
	1	2	3	4	
1	On	On	On	On	1024x768 Dual Scan STN Color Panel
2	Off	On	On	On	1280x1024 TFT Color Panel
3	On	Off	On	On	640x480 Dual Scan STN Color Panel
4	Off	Off	On	On	800x600 Dual Scan STN Color Panel
5	On	On	Off	On	800x600 Sharp Color Panel
6	Off	On	Off	On	640x480 18-bit Color Panel
7	On	Off	Off	On	1024x768 TFT Color Panel
8	Off	Off	Off	On	800x600 TFT Color Panel
9	On	On	On	Off	800x600 TFT Color Pane
10	Off	On	On	Off	800x600 TFT Color Panel
11	On	Off	On	Off	800x600 Dual Scan STN Color Panel
12	Off	Off	On	Off	800x600 Dual Scan STN Color Panel
13	On	On	Off	Off	1024x768 TFT Color Panel
14	Off	On	Off	Off	1280x1024 Dual Scan STN Color Panel
15	On	Off	Off	Off	1024x600 Dual Scan STN Color Panel
16	Off	Off	Off	Off	1024x600 TFT Color Pane

Chapter 4 SRAM Disk

The section describes the various types of solid-state disk. The following topics are covered:

- Overview
- Switch Setting
- Programming SRAM Disk

OVERVIEW

The FB2502 provides one DIP socket and two SMD SRAM, which may be populated with up to 0.5 /1.5 MB of SRAM or DiskOnChip up to 288MB. It is ideal for diskless systems, high reliability and/or high-speed access applications, controller for industrial or line test instruments, and etc.

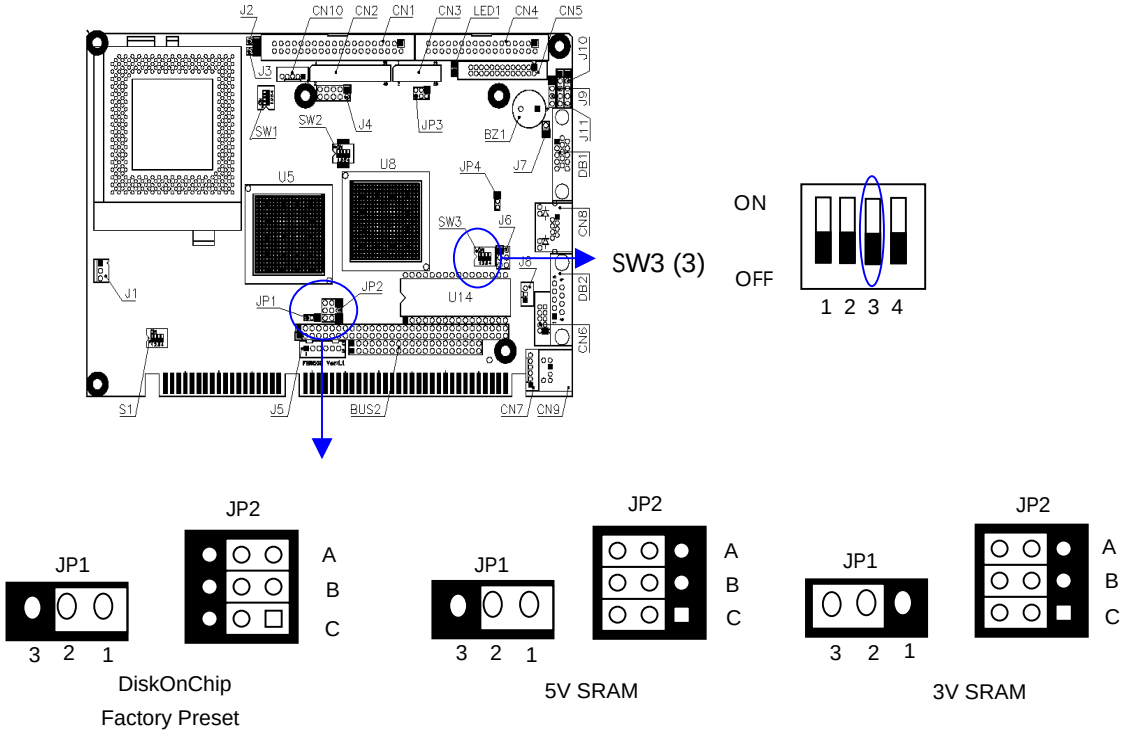
SRAM disk function allows you to directly program the SRAM disk without having to purchase any additional programming equipment. You could format SRAM disk and copy files onto SRAM disk just like using a normal floppy and hard disk. You can use all of the related DOS command (such as COPY, DEL...etc.) to update files on SRAM disk.

Switch Setting

SRAM /D.O.C. DISK Select

SW3 (3): DiskOnChip / SRAM Mapping Address Select

If DiskOnChip or SARM is to be used, select a mapping memory address for it. Two addresses are provided, CC00, D800. The default setting is CC00.



SW3-3	SRAM Disk Memory Bank Segment (8K)	SSD BIOS Memory Bank Segment (16K)	Remark
Off	CE00:0	DC00:0	Default
On	DA00:0	DC00:0	

Note1: If SSD Disk enable, the system will be reserved 32K byte

Note2: If a SRAM is installed to the system, The BIOS CMOS SETUP is determined by select 68h or 78h.

SSD Memory Type Select (Switch 1-1 & 1-2)

The Switch 3-3 is used to select the memory bank segment. You must select an appropriate memory bank segment so that the FB2502 will not conflict with memory installed on other add-on memory cards. Additionally, be sure not to use shadow RAM area or EMM driver's page frame in this area.
If you are not going to use the SRAM Disk, you can use BIOS setup program to disable the SRAM BIOS. The FB2502 will not occupy any memory address if the SRAM BIOS is disabled.

If you are going to install the EMM386.EXE driver, please use the [X] option to prevent EMM386.EXE from using the particular range of segment address as an EMS page, which is used by FB2502. For example, write a statement in the CONFIG.SYS file as follow: (If the memory configuration of FB2502 is CE00:0)

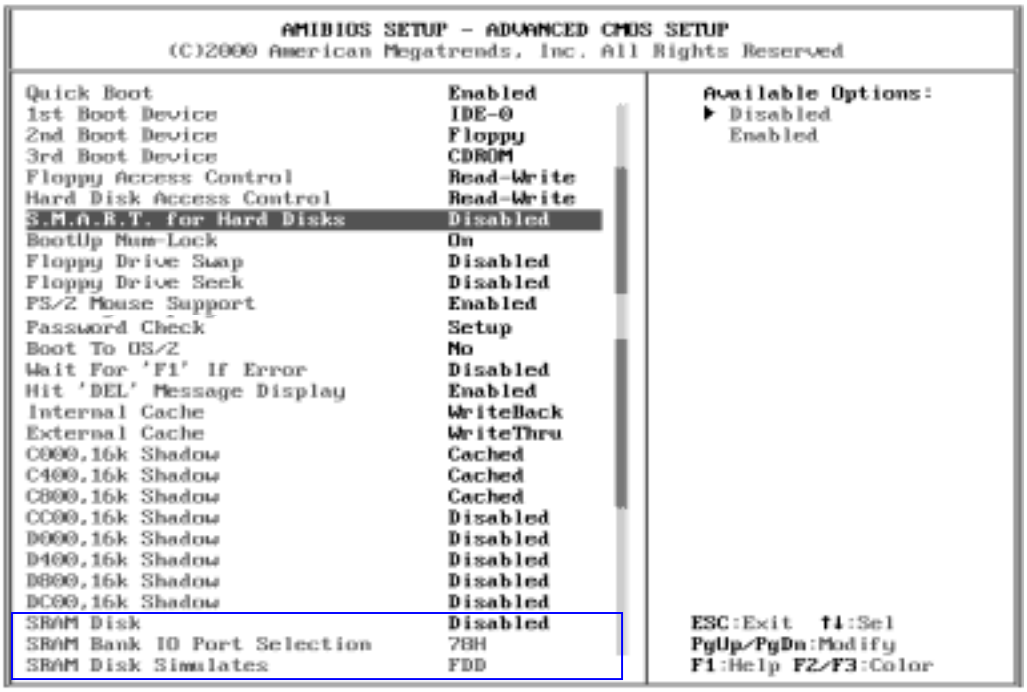
DEVICE=C:\DOS\EMM386.EXE X=CE00-CFFF

Programming SRAM Disk

The sample procedure is step by step for SSD is below:

Programming SSD (Floppy)

1. Install the flash in Socket U10.
2. Set the JP1&JP2 and SW3 - 3 to SRAM position (The SSD data bank is CE00:0)
3. Connect power to the system.
4. Power ON.
5. Press Delete key to display the BIOS Setup menu.
6. Enter CMOS Setup menu. Then choice to CMOS SET UP >ADVANCE CMOS SETUP >SRAM DISK set to ENABLE
7. In the SRAM Disk Simulates field, select FDD that the SRAM disk will act a physical floppy disk. Then, save the setting. (The system will be restart) the screen like below:



8. On the screen, use the up or down arrow keys to select a flash type and size.

   The screen like below:

   FB2502 SSD BIOS version 1.20 (c) 2001 FabiaTech Corp

   SRAM Disk Setting: Disk B: Unknow??? ..512K Maximum

   Base Port Address : 0078h Firmware Seg.: DC00h Data Bank Seg.: CE00h

   DOS Booting Driver : As BIOS Setting M1(U14) Socket Setting: SSD

9. The booting from other device. (Like physical FDD)

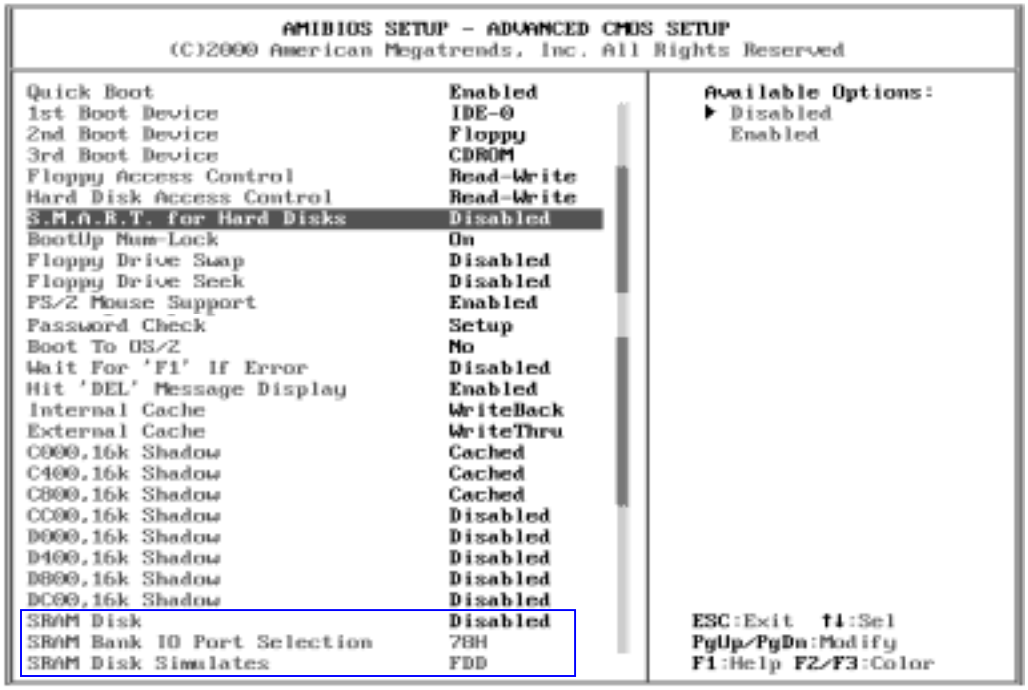
10. Use the FORMAT command to format the flash disk in DOS mode. (This time this SSD is B:)

11. Use FORMAT B:/S /C/ U (The S: SYSTEM BOOTING /C: Check /U: UNFORMAT

    If format parameterize no " /S " the SSD will be always to device B: that can't booting the system.

Programming SSD (HDD)

1. Install the flash disk in Socket U10
2. Set the JP1&JP2 and SW3-3 to off position (The SSD data bank is CE00:0)
3. Connect power to the system.
4. Power ON.
5. Press Delete key to display the BIOS Setup menu.
6. Enter the CMOS Setup menu. Then choice to CMOS SET UP >ADVANCE CMOS SETUP SSD FUNCTION ENABLE
7. In the SRAM Disk Simulates field, select HDD that the flash disk will act as a physical hard disk. Then, save the setting. The screen like below:



8. On the screen, use the up or down arrow keys to select a flash type and size.

The screen like below:

FB2502 SSD BIOS version 1.20 (c) 2001 FabiaTech Corp

SRAM Disk Setting : Disk #80h (C:) Unknow ??? ..512K Maximum

Base Port Address: 0078h Firmware Seg.: DC00h Data Bank Seg.: CE00h

DOS Booting Driver : As BIOS Setting M1(U14) Socket Setting: SSD

9. The booting from other device. (Like physical HDD)

10. Set the FDISK command to partition the flash disk in DOS mode. (If system is not physical HDD the SSD is C:)

11. Use FORMAT C:/S /C/ U (The S: SYSTEM BOOTING /C: Check /U: UNFORMAT)

    If format parameter no " /S " the SSD will be can't boot the system.

Note: 1.If SRAM Disk Simulates field select HDD, The SRAM disk total size must be above to 512KB.

2.An on-board Lithium battery or an external battery pack that could be connected ensures data retention of SRAM to the FB2502.

Chapter 5 BIOS Setup

This chapter describes the BIOS setup.

Overview

BIOS are a program located on a Flash memory chip on a circuit board. It is used to initialize and set up the I/O peripherals and interface cards of the system, which includes time, date, hard disk drive, the ISA bus and connected devices such as the video display, diskette drive, and the keyboard. This program will not be lost when you turn off the system.

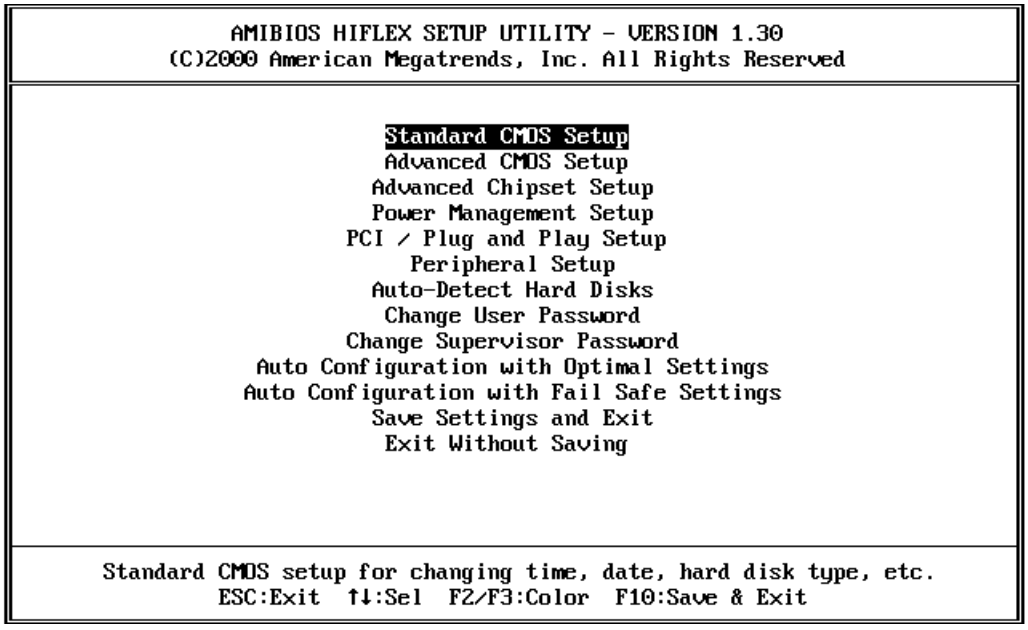
The BIOS provides a menu-driven interface to the console subsystem. The console subsystem contains special software, called firmware that interacts directly with the hardware components and facilitates interaction between the system hardware and the operating system.

The BIOS default values ensure that the system will function at its normal capability. In the worst situation the user may have corrupted the original settings set by the manufacturer.

All the changes you make will be saved in the system RAM and will not be lost after power-off.

When you start the system, the BIOS will perform a self-diagnostics test called Power On Self Test (POST) for all the attached devices, accessories, and the system. Press the [Del] key to enter the BIOS Setup program, and then the main menu will show on the screen.

Note: Change the parameters when you fully understand their functions and subsequence.


AMIBIOS HIFLEX SETUP UTILITY - VERSION 1.30
(C)2000 American Megatrends, Inc. All Rights Reserved
Standard CMOS Setup
Advanced CMOS Setup
Advanced Chipset Setup
Power Management Setup
PCI / Plug and Play Setup
Peripheral Setup
Auto-Detect Hard Disks
Change User Password
Change Supervisor Password
Auto Configuration with Optimal Settings
Auto Configuration with Fail Safe Settings
Save Settings and Exit
Exit Without Saving
Standard CMOS setup for changing time, date, hard disk type, etc.
ESC:Exit ↑↓:Sel F2/F3:Color F10:Save & Exit

BIOS Functions

On the menu, you can perform the following functions

1. Standard CMOS Setup- Advanced CMOS Setup
2. Advanced Chipset Setup
3. Power Management Setup
4. PCI/ Plug and Play Setup
5. Peripheral Setup
6. Hardware Monitor Setup
7. Auto-Detect Hard Disks
8. Change User Password
9. Change Supervisor Password
10. Auto Configuration with Optimal Settings: to auto configure the system according to optimal setting with pre-defined values. This is also the factory default setting of the system when you receive the board.
11. Auto Configuration with Fail Safe Settings: to configure the system in fail-safe mode with predefined values.
12. Save Settings and Exit: perform this function when you change the setting and exit the BIOS Setup program.
13. Exit without saving: perform this function when you want to exit the program and do not save the change.

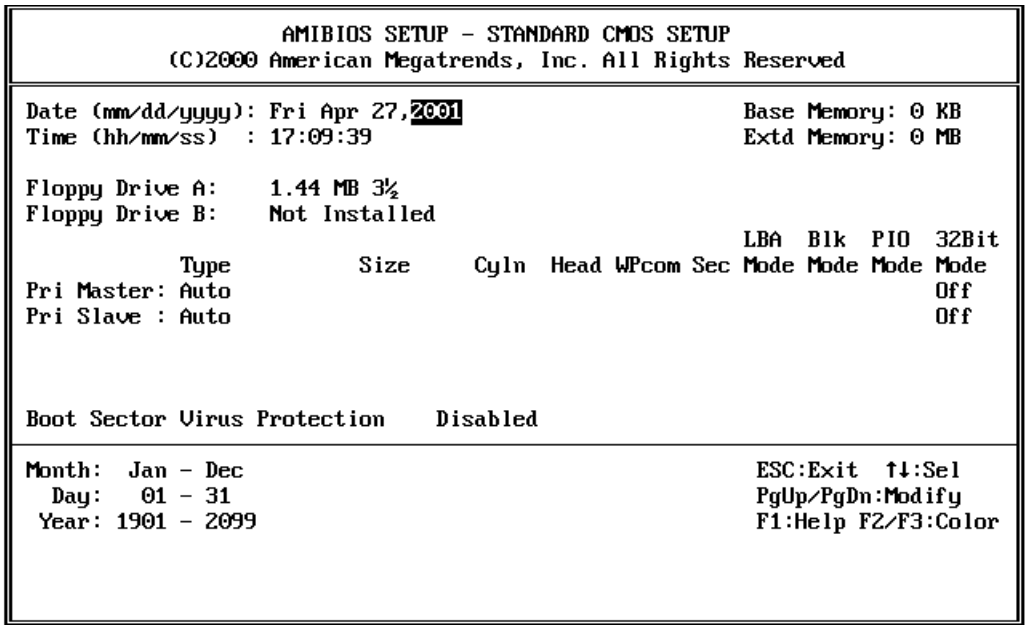
Keyboard Convention

On the BIOS, the following keys can be used to operate and manage the menu:

Item	Function
ESC	To exit the current menu or message
Page Up/Page Down	To select a parameter
F1	To display the help menu if you do not know the purpose or function of the item you are going to configure
F2/F3	To change the color of the menu display. F2 is to go forward and F3 is to go backward
UP/Down Arrow Keys	To go upward or downward to the desired item

STANDARD CMOS SETUP

This section describes basic system hardware configuration, system clock setup and error handling. If the CPU board is already installed in a working system, you will not need to select this option anymore.


AMIBIOS SETUP - STANDARD CMOS SETUP
(C)2000 American Megatrends, Inc. All Rights Reserved
Date (mm/dd/yyyy): Fri Apr 27,2001
Time (hh/mm/ss) : 17:09:39
Base Memory: 0 KB
Extd Memory: 0 MB
Floppy Drive A: 1.44 MB 3½
Floppy Drive B: Not Installed
Type Size Cyln Head WPcom Sec LBA Mode Blk Mode PIO Mode 32Bit Mode
Pri Master: Auto Off
Pri Slave : Auto Off
Boot Sector Virus Protection Disabled
Month: Jan - Dec
Day: 01 - 31
Year: 1901 - 2099
ESC:Exit ↑↓:Sel
PgUp/PgDn:Modify
F1:Help F2/F3:Color

- **Date & Time Setup**

Highlight the <Date> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the month, day and year format.

Highlight the <Time> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the hour, minute and second format.

The user can bypass the date and time prompts by creating an AUTOEXEC.BAT file. For information on how to create this file, please refer to the MS-DOS manual.

- **Floppy Setup**

The <Standard CMOS Setup> option records the types of floppy disk drives installed in the system.

To enter the configuration value for a particular drive, highlight its corresponding field and then select the drive type using the left-or right-arrow key.

- **Hard Disk Setup**

The BIOS supports various types for user settings, The BIOS supports <Pri Master>, <Pri Slave>, <Sec Master> and <Sec Slave> so the user can install up to four hard disks. For the master and slave jumpers, please refer to the hard disk's installation descriptions and the hard disk jumper settings.

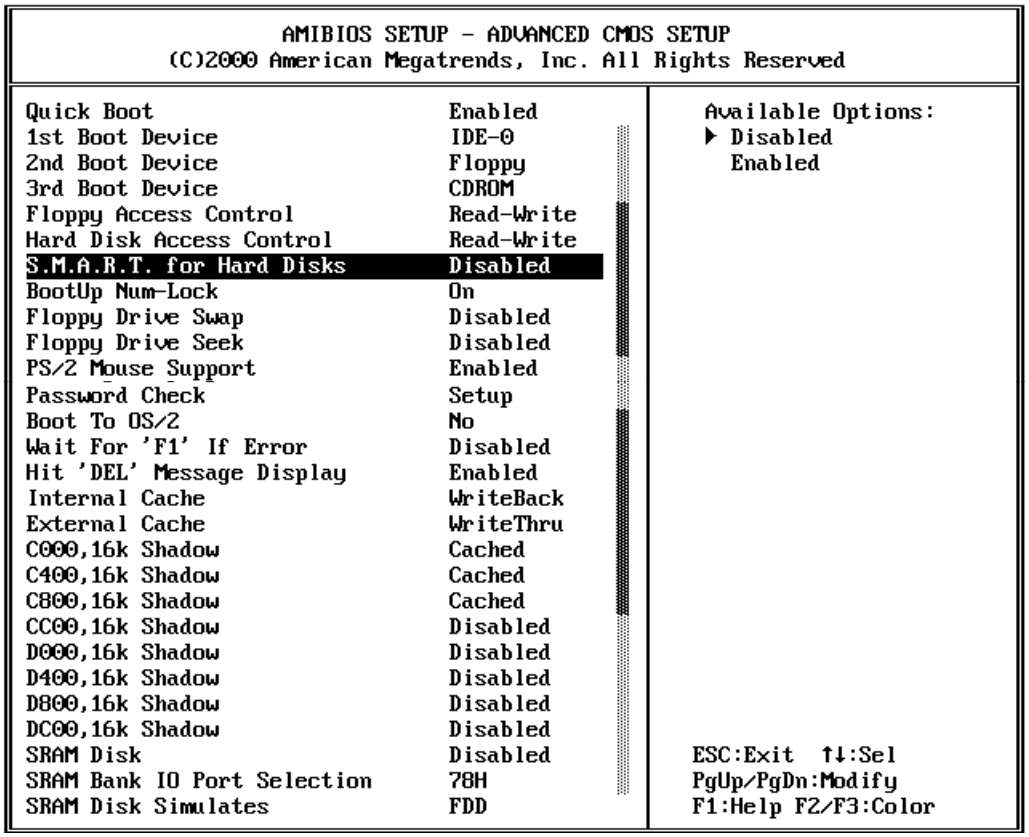
You can select <AUTO> under the <TYPE> and <MODE> fields. This will enable auto detection of your IDE drives during boot up. This will allow you to change your hard drives (with the power off) and then power on without having to reconfigure your hard drive type. If you use older hard disk drives, which do not support this feature, then you must configure the hard disk drive in the standard method as described above by the <USER> option.

- **Boot Sector Virus Protection**

This option protects the boot sector and partition table of your hard disk against accidental modifications. Any attempt to write to them will cause the system to halt and display a warning message. If this occurs, you can either allow the operation to continue or use a bootable virus-free floppy disk to reboot and investigate your system. The default setting is <***Disabled***>. This setting is recommended because it conflicts with new operating systems. Installation of new operating system requires that you disable this to prevent write errors.

ADVANCED CMOS SETUP

This section describes the configuration entries that allow you to improve your system performance, or let you set up some system features according to your preference. Some entries here are required by the CPU board's design to remain in their default settings.



- **Quick Boot**

This field is used to activate the quick boot function of the system. When set to Enabled,

1. BIOS will not wait for up to 40 seconds if a Ready signal is not received from the IDE drive, and will not configure its drive.

2. BIOS will not wait for 0.5 seconds after sending a RESET signal to the IDE drive.

3. You cannot run BIOS Setup at system boot since there is no delay for the Hit, Del. To run Setup message.

Available Options: Disabled, Enabled

Default setting: Enabled

- **1st –3rd Boot Device**

These fields determine where the system attempts to look for the boot drive priority for an operating system. The default procedure is to check the hard disk, and then the floppy drive, and last the CDROM.

Available options: Disabled, IDE0-1, IDE-2, IDE-3, Floppy, ARMD-FDD, ARMD-HDD, CDROM, and SCSI, Network

Default setting: IDE-0 for 1st Boot device; Floppy for 2nd Boot Device; CDROM for 3rd Boot Device

- **Floppy Access Control**

This field specifies the read/write access when booting from a floppy drive.

Available options: Normal, Read-only

Default setting: Normal

- **Hard Disk Access Control**

This field specifies the read/write access when booting from a HDD drive.

Available options: Normal, Read-only

Default setting: Normal

- **S.M.A.R.T for Hard Disk**

This field is used to activate the S.M.A.R.T (System Management and Reporting Technologies) function for S.M.A.R.T HDD drives. This function requires an application that can give S.M.A.R.T message.

Available options: Disabled, Enabled

Default: Disabled

- **Boot Up Numlock**

This field is used to activate the Num Lock function upon system boot. If the setting is on, after a boot, the Num Lock light is lit, and user can use the number key.

Available options: On, Off

Default setting: On

- **Floppy Drive Swap**

The field reverses the drive letter assignments of your floppy disk drives in the Swap A, B setting, otherwise leave on the default setting of ***Disabled*** (No Swap). This works separately from the BIOS Features floppy disk swap feature. It is functionally the same as physically interchanging the connectors of the floppy disk drives. When the function's setting is <***Enabled***>, the BIOS swapped floppy drive assignments so that Drive A becomes Drive B, and Drive B becomes Drive A under DOS.

Available options: Disabled, Enabled

Default setting: Disabled

- **Floppy Drive Seek**

This field is used to set if the BIOS will seek the floppy <A> drive upon boot.

Available Options: Disabled, Enabled

Default setting: Disabled

- **PS/2 Mouse Support**

The PS/2 mouse function is optional. Before you configure this field, make sure your FB2502 supports this feature. The setting of ***Enabled*** allows the system to detect a PS/2 mouse on boot up. If detected, IRQ12 will be used for the PS/2 mouse. IRQ 12 will be reserved for expansion cards if a PS/2 mouse is not detected. ***Disabled*** will reserve IRQ12 for expansion cards and therefore the PS/2 mouse will not function.

Available options: Disabled, Enabled

Default setting: Enable

- **Typematic rate**

This function specifies the keystroke repeat rate when a key is pressed and held down.

Available options: Fast, Slow

Default setting: Fast

- **System Keyboard**

This field specifies if an error message should be prompted when a keyboard is not attached.

Available options: Absent, Present

Default setting: Absent

- **Primary Display**

The field specifies the type of monitor installed in the system.

Available options: Absent, VGA/EGA, CGA40x25, CGA80x25, and Mono

Default setting: Absent

- **Password Check**

This field enables password checking every time the computer is powered on or every time the BIOS Setup is executed. If ***Always*** is chosen, a user password prompt appears every time and the BIOS Setup Program executes and the computer is turned on. If ***Setup*** is chosen, the password prompt appears if the BIOS executed.

Available options: Setup, Always

Default setting: Setup

- **Boot To OS2> 64MB**

If OS2 operating system is used, and the system RAM is over 64MB, please select yes. Otherwise, select No.

Available options: Yes, No

Default setting: No

- **Wait for 'F1' If Error**

AMIBIOS POST error messages are followed by:

```
Press <F1> to continue
```

If this field is set to ***Disabled***, the AMIBIOS does not wait for you to press the <F1> key after an error message.

Available options: Disabled, Enabled

Default setting: Disabled

- **Hit 'DEL' Message Display**

Set this field to ***Disabled*** to prevent the message as follows:

```
Hit 'DEL' if you want to run setup
```

It will prevent the message from appearing on the first BIOS screen when the computer boots.

Available options: Disabled, Enabled

Default setting: Enabled

- **C000, 32k Shadow - E800, 32k shadow**

These fields control the location of the contents of the 32KB of ROM beginning at the specified memory location. If no adapter ROM is using the named ROM area, this area is made available to the local bus. The settings are:

1. **Disabled:** The video ROM is not copied to RAM. The contents of the video ROM cannot be read from or written to cache memory.

2. **Enabled:** The contents of C000h - C7FFFh are written to the same address in system memory (RAM) for faster execution.

3. **Cached**: The contents of the named ROM area are written to the same address in system memory (RAM) for faster execution, if an adapter ROM will be using the named ROM area. Also, the contents of the RAM area can be read from and written to cache memory.

Available options: Disabled, Enabled, Cached

Default setting: Disabled

- **SRAM Disk**

These fields control the location of the contents of the solid-state disk beginning.

Available Options: Disable, D000, D800, E000 and E800.

Default setting: Disable

- **SRAM Bank IO Port Select**

This field specifies the Select SRAM IO port, if a SRAM is installed to the system. If Disabled are selected, the system will not be able to use SRAM.

Available Options: Disable, 78h, and 68h

Default setting: Disable

- **SRAM Simulates**

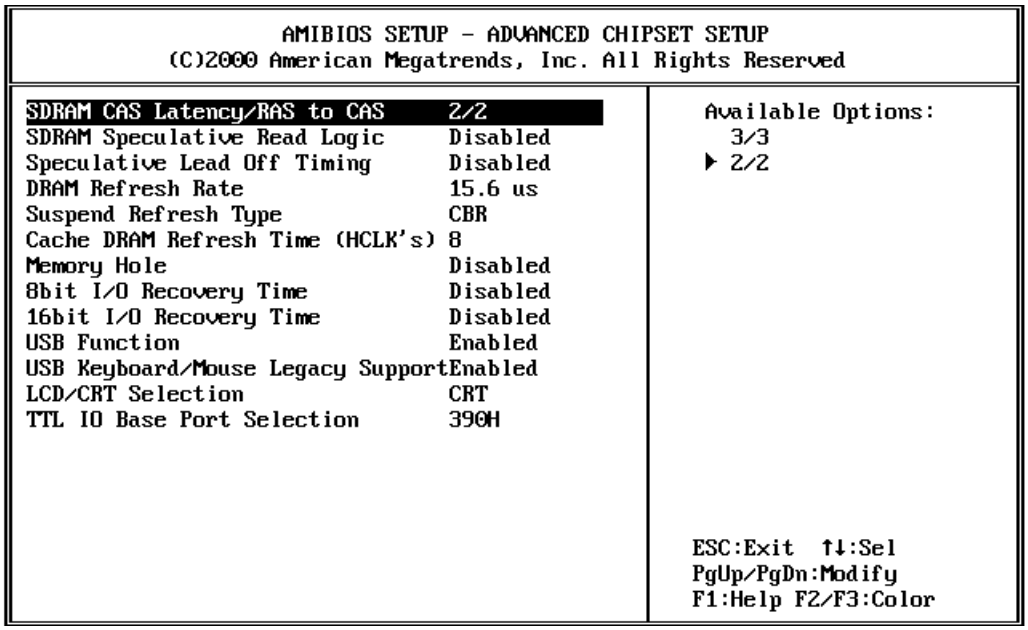
When HDD is selected, the system will boot from the SRAM as if it is a hard disk drive. When FDD is selected, the system will boot from the SRAM as if it is a floppy disk drive (a:).

Available Options: HDD, FDD

Default setting: HDD

ADVANCED CHIPSET SETUP

This section describes the configuration of the board's chipset features.


AMIBIOS SETUP - ADVANCED CHIPSET SETUP
(C)2000 American Megatrends, Inc. All Rights Reserved
SDRAM CAS Latency/RAS to CAS 2/2
SDRAM Speculative Read Logic Disabled
Speculative Lead Off Timing Disabled
DRAM Refresh Rate 15.6 us
Suspend Refresh Type CBR
Cache DRAM Refresh Time (HCLK's) 8
Memory Hole Disabled
8bit I/O Recovery Time Disabled
16bit I/O Recovery Time Disabled
USB Function Enabled
USB Keyboard/Mouse Legacy Support Enabled
LCD/CRT Selection CRT
TTL IO Base Port Selection 390H
Available Options:
3/3
▶ 2/2
ESC:Exit ↑↓:Sel
PgUp/PgDn:Modify
F1:Help F2/F3:Color

- **SDRAM CAS Latency/RAS to CAS**

This field specifies the length of the delay inserted between RAS and CAS signals of the Synchronous DRAM system access cycle when SDRAM is installed.

Available Options: 3/3 SCLKS, 2/2 SCLKS

Default setting: 2/2 SCLKS

- **SDRAM Speculative Read Logic**

This field specifies the length of the RAS precharge part of the Synchronous DRAM access cycle when SDRAM is installed.

Available Options: Disable, Enable

Default setting: Disable

- **SDRAM Speculative Lead Off Timing**

This field specifies the DRAM Controller read request is presented before the final memory target.

Available Options: Disable, Enable

Default setting: Disable

- **DRAM Refresh Rate**

This specifies the DRAM refresh rate.

Available Options: 15.6 us, 31.2 us, 62.4 us, 124.8 us, and 249.6 us

Default setting: 15.6 us

- **Memory Hole**

This field specifies the location of an area of memory that cannot be addressed on the ISA bus.

Available Options: Disabled, 15MB-16MB, 512KB-64KB

Default setting: Disabled

- **8bit I/O Recovery Time**

The recovery time is the length of time, measured in CPU clocks, which the system will delay after achieving an input/output request. This delay takes place to wait for the I/O to complete the request. This field specifies the recovery time for 8bit I/O.

Available Options: Disabled, 1 – 8 Sysclk

Default setting: Disabled

- **16Bit I/O Recovery Time**

This field specifies the recovery time for 16Bit I/O.

Available Options: Disabled, 1 – 4 Sysclk

Default setting: Disabled

- **USB Function**

Select Enabled if a USB device is installed to the system. If Disabled are selected, the system will not be able to use a USB device.

Available Options: Disabled, Enabled

Default setting: Enabled

- **LCD CRT Selection**

This item configures to the incorrect display setting. Can viewing LCD or CRT and BOTH If CRT are selected, the system will be only CRT display.

Available Options: LCD, CRT, and BOTH

Default setting: CRT

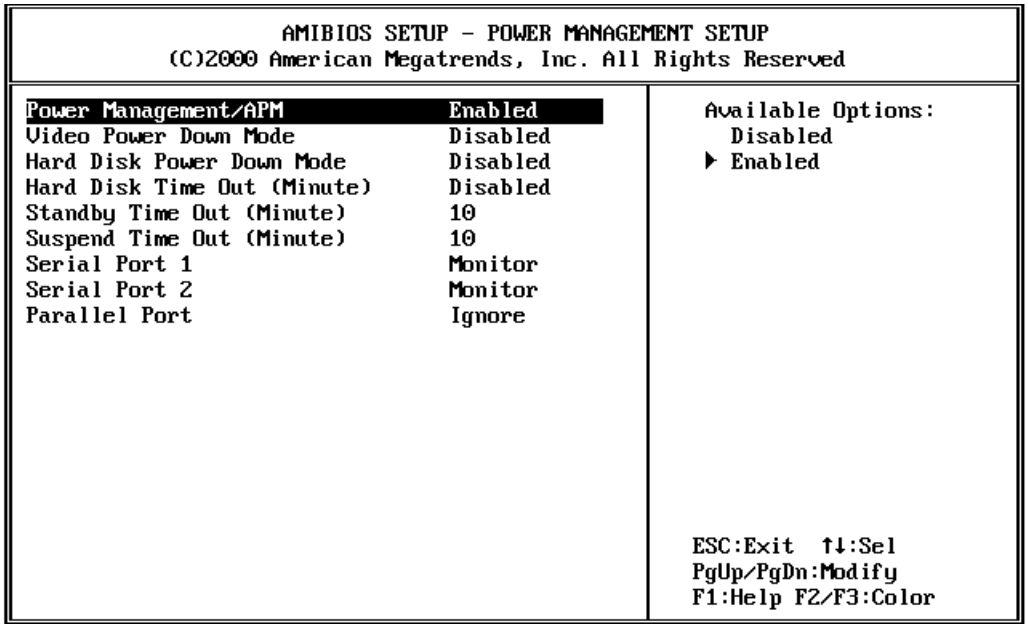
- **TTL IO Base port Selection**

This field specifies the Select IO port for CN11, if an I/O is select to the system. If Disabled are selected, the system will not be able to use I/O.

Available Options: Disable, 190h, 290h and 390h

Default setting: Disable

POWER MANAGEMENT



- **Power Management /APM**

Select Enabled to activate the chipset Power Management and APM (Advanced Power Management) features.

Available Options: Disabled, Enabled

Default setting: Disabled

- **Video Power Down Mode**

This field specifies the power conserving state that video subsystem enters after the specified period of display inactivity has expired.

Available Options: Disabled, Standby, Suspend

Default setting: Disabled

- **Hard Disk Power Down Mode**

This field specifies the power conserving state that the hard disk drive enters after the specified period of hard drive inactivity has expired.

Available Options: Disabled, Standby, Suspend

Default setting: Disabled

- **Hard Disk Time Out (Minute)**

This field specifies the length of period of hard disk inactivity. When this period has expired, the system enters power-conserving state specified in the HARD DISK POWER DOWN MODE field.

Available Options: Disable, 1 min (minute), 2 min, 3 min, 4 min, 5 min, 6 min, 7 min, 8 min, 9 min, 10 min, 11 min, 12 min, 13 min, 14 min, and 15 min.

Default setting: Disabled

- **Standby Time Out (Minute)**

This field specifies the length of a period of system inactivity (like hard disk or video) while in full power on state. When this length of time expires, the system enters Standby power state.

Available Options: Disabled, 1 Minute, 2 Minute, 4 Minute, and 8 Minute, up to 60 Minute.

Default setting: Disabled

- **Suspend Time Out (Minute)**

This field specifies the length of a period of system inactivity (like hard disk or video) while in Standby state. When this length of time expires, the system enters Suspend power state.

Available Options: Disabled, 1 Minute, 2 Minute, 4 Minute, and 8 Minute, up to 60 Minute.

Default setting: Disabled

- **Serial port 1**

This field specifies the power down mode of the system based on the device connected to COM1. When the system does not receive signals from the COM1, it will enter the Power Down mode immediately. To enable the power saving mode, select Monitor. To disable it, select Ignore.

Available Options: Monitor, Ignore

Default setting: Monitor

- **Serial port 2**

This field specifies the power down mode of the system based on the device connected to COM2. When the system does not receive signals from the COM2, it will

enter the Power Down mode immediately. To enable the Power Down mode, select Monitor. To disable it, select Ignore.

Available Options: Monitor, Ignore

Default setting: Monitor

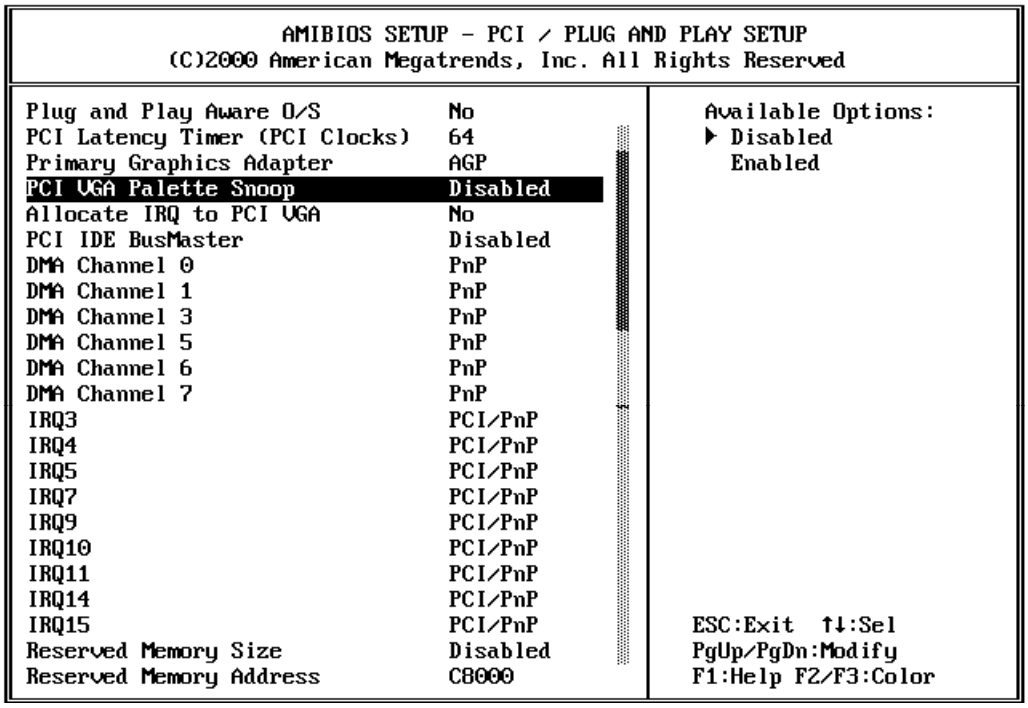
- **Parallel port**

This field specifies the power down mode of the system based on the device connected to the parallel port. When the system does not receive signals from the parallel port, it will enter the Power Down mode immediately. To enable the Power Down mode, select Monitor. To disable it, select Ignore.

Available Options: Monitor, Ignore

Default setting: Ignore

PCI/PLUG AND PLAY



- **Plug and Plug Aware O/S**

Set to yes to inform BIOS that the operating system can handle Plug and Play (PnP) devices.

Available Options: Yes, No

Default setting: No

- **PCI Latency Timer**

This field specifies the latency timings (in PCI clock) PCI devices installed in the PCI expansion bus.

Available Options: 32, 64, 96, 128, 160,192, 224, and 248

Default setting: 64

- **PCI VGA Palette Snoop**

When Enabled is selected, multiple VGA devices operating on different buses can handle data from the CPU on each set of palette registers on every video device. Bit

5 of the command register in the PCI device configuration space is the VGA Palette Snoop bit. (0 is disabled).

Available Options:

Disabled: Data read and written by the CPU is only directed to the PCI VGA devices palette registers.

Enabled: Data read and written by the CPU is directed to both the PCI VGA device's palette registers and the ISA VGA device palette registers, permitting the palette registers of both devices to be identical.

Default setting: Disable

- **Allocate IRQ to PCI AGP**

When a PCI or AGP VGA device is installed, you can assign an IRQ to this device. Selecting Yes, BIOS will auto-assign IRQ to the device. Selecting No, no IRQ will be assigned to the VGA device.

Available Options: Yes, No

Default setting: No

- **PCI IDE BusMaster**

This option is to specify that the IDE controller on the PCI local bus have bus-mastering capability.

Available Options: Enable, Disable

Default setting: Disable

- **DMA Channel 0 – 7**

When I/O resources are controlled manually, you can assign each system DMA as one of the following types, based on the type of device using the interrupt:

ISA/EISA devices comply with the original PC AT bus specification, requiring a specific interrupt (Such as IRQ5 for COM1).

PnP (PCI/ISA) devices: comply with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

Available Options: PnP, ISA/EISA

Default setting: PnP

- **IRQ 3 –15**

When I/O resources are controlled manually, you can assign each system interrupt as one of the following types, based on the type of device using the interrupt:

ISA/EISA devices comply with the original PC AT bus specification, requiring a specific interrupt (Such as IRQ5 for COM1).

PnP (PCI/ISA) devices: comply with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

- **Reserved Memory Size**

You can manually reserve a memory size for a certain interface card if required.

Available Options: Disabled, 16K, 32K, 64K

Default setting: Disabled

- **Reserved Memory Address**

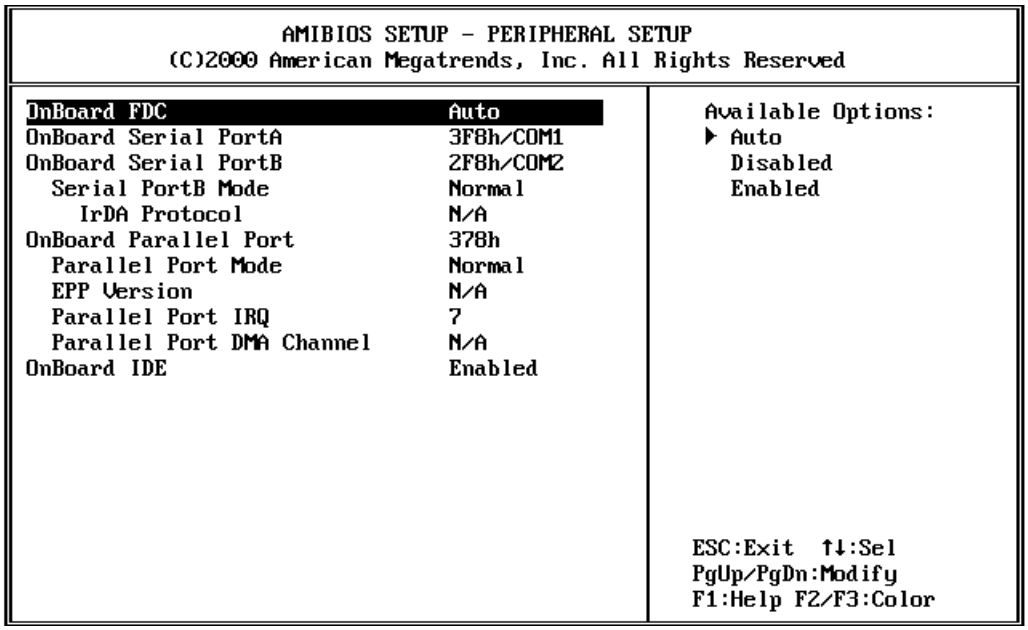
When a memory Reserved Memory Size is enabled, specify an address range within the C8000 and DC000.

Available Options: C0000, C4000, C8000, CC000, D0000, D4000, D8000, DC000.

Default setting: C8000

PERIPHERAL SETUP

This section describes the function of peripheral features.



- **OnBoard FDC**

This field enables the floppy drive controller on the FB2502.

Available Options: Disabled, Enabled

Default setting: Enabled

- **OnBoard Serial Port A**

These fields select the I/O port address for each Serial port. Refer to Table 2-2.

Available Options: Auto, Disabled, 3F8H/COM1, 2F8H/COM2, and 3E8H/COM3, 2E8H/COM4.

Default setting: 3F8H/COM1

- **OnBoard Serial Port B**

These fields select the I/O port address for each Serial port. Refer to Table 2-2.

Available Options: Auto, Disabled, 3F8H/COM1, 2F8H/COM2, and 3E8H/COM3, 2E8H/COM4.

Default setting: 2F8H/COM2

- **Serial Port B Mode**

COMB can be configured for either IR or COM port application. Normal is

Available Options: Normal, IrDA, ASK IR

Default setting: Normal

- **IrDA Protocol**

When IrDA or ASK IR is selected on the above Serial Port B Mode, you can select 1.6 us or 3/16 us. When Normal is selected, this field displays N/A and cannot be configured.

Available Options: N/A, 1.6 us, 3/16 us

Default setting: N/A

- **OnBoard Parallel Port**

This field selects the I/O port address for parallel port.

Available Options: Auto, Disabled, 378, 278, and 3BCH

Default setting: 378H

- **Parallel Port Mode**

This field specifies the parallel port mode. ECP and EPP are both bi-directional data transfer schemes that adhere to the IEEE P1284 specifications.

Available Options: N/A, Normal, Bi-Dir, EPP, and ECP

Default setting: Normal

- **EPP Version**

This field specifies the EPP version for the Parallel Port Mode specification used in the system and is not configurable. IF Normal or ECP is selected, this field displays N/A, meaning not available.

Available Options: N/A, 1.7, 1.9

Default setting: N/A

- **Parallel Port IRQ**

This field specifies the IRQ for the parallel port.

Available Options: Auto, N/A, 5, 7

Default setting: IRQ7 for Parallel Port; IRQ5 for Parallel Port 2

- **Parallel Port DMA Channel**

This option is only available if the setting for the parallel Port Mode option is ECP.

Available Options: N/A, 0,1,3

Default setting: N/A

- **OnBoard IDE**

This field specifies the IDE channel that can be applied when using CN3 IDE hard disk connector.

Available Options: Disabled, Primary, and Secondary, Both

Default setting: Primary

Password Setup

There are two security passwords: Supervisor and User. Supervisor is a privileged person that can change the User password from the BIOS.

According to the default setting, both access passwords are not set up and are only valid after you set the password from the BIOS.

To set the password, please complete the following steps.

1. Select **Change Supervisor Password.**
2. Type the desired password (up to 8 character length) when you see the message, "Enter New Supervisor Password."
3. Then you can go on to set a user password (up to 8 character length) if required. Note that you cannot configure the User password until the Supervisor password is set up.
4. Enter Advanced CMOS Setup screen and point to the Password Checkup field.
5. Select Always or Setup.

✧ **Always:** a visitor who attempts to enter BIOS or operating system will be prompted for password.

✧ **Setup:** a visitor who attempts to the operating system will be prompted for user password. You can enter either User password or Supervisor password.

6. Point to **Save Settings and Exit** and press Enter.
7. Press Y when you see the message, "Save Current Settings and Exit (Y/N)?"

Note: it is suggested that you write down the password in a safe place to avoid that password may be forgotten or missing.

To set the password, please complete the following steps.

1. Select **Change Supervisor Password**.
2. Press Enter instead of entering any character when you see the message, "Enter New Supervisor Password."
3. Thus you can disable the password.

Chapter 6 Driver and Utility

The enclosed diskette includes FB2502 VGA and LAN driver.

VGA Driver for Win 31

Step 1: To install the VGA driver, insert the CD ROM into the CD ROM device, and enter DRIVER>VGA>CT69000>WIN31. If your system is not equipped with a CD ROM device, copy the VGA driver from the CD ROM to a 1.44" diskette.

Step 2: Execute setup.exe file.

Step 3: The screen shows the chip type. Press any key to enter the main menu.

Step 4: There are some items for choice to setup. Please choose the <Windows Version 3.1> item notice the function key defined. Press [ENTER] selected the <All Resolutions>, when this line appears [*] symbol, which means this item is selected. Pressing [End] starts to install.

Step 5: The screen will show the dialog box, demanding the user to type the WIN31's path. The default is C:\WINDOWS.

Step 6: As the setup is completed, the system will generate the message as follows.

Installation is done!

Change to your Windows directory and type SETUP to run the Windows Setup program. Choose one of the new drivers marked by an *. Please refer to the User's Guide to complete the installation.

Step 7: Press the [Esc] key to return to the main menu, and re-press the [Esc] key to return to the DOS mode.

Step 8: In the WIN31, you can find the <Chips CPL> icon located in the {CONTROL PANEL} group.

Step 9: Adjust the <Refresh Rate>, <Cursor Animation>, <Font size>, <Resolution>, and <Big Cursor>.

WIN98/WIN95 Driver

1 To install the VGA driver, insert the CD ROM into the CD ROM device, and enter DRIVER>VGA>CT69000>WIN98. If your system is not equipped with a CD ROM device, copy the VGA driver from the CD ROM to a 1.44" diskette.

2 Execute setup.exe file.

3 The screen shows the SETUP type. Press any key to enter the main menu.

4 As the setup is completed, the system will generate the message as follows.

Yes, I want to restart my computer now. Installation is done!

No, I will restart my computer later.

System must be restart then complete the installation.

7 In the WINDOWS98/ME, you can find the <DISPLAYL> icon located in the {CONTROL PANEL} group.

8 Adjust the <Refresh Rate>, <Cursor Animation>, <Font size>, <Resolution>, and <Big Cursor>.

Note: In the VGA>CT69000>NT4.0 or OS2 directory, a Install.txt/Readme.txt file is included to provide installation information

BIOS Flash Utility

In the <UTILITY> directory, there is the FLASH818.EXE file.

Step 1: Use the AMIFLASH.COM program to update the BIOS setting.

Step 2: And then refer to the chapter "BIOS Setup", as the steps to modify BIOS.

Step 3: Now the CPU board's BIOS loaded with is the newest program; user can use it to modify BIOS function in the future, when the BIOS add some functions.

LAN Utility

Step 1: To install the LAN utility OR driver, insert the CD ROM into the CD ROM device, and enter DRIVER>LAN>RTL8139C>DIAG. If your system is not equipped with a CD ROM device, copy the LAN VGA driver from the CD ROM to a 1.44" diskette.

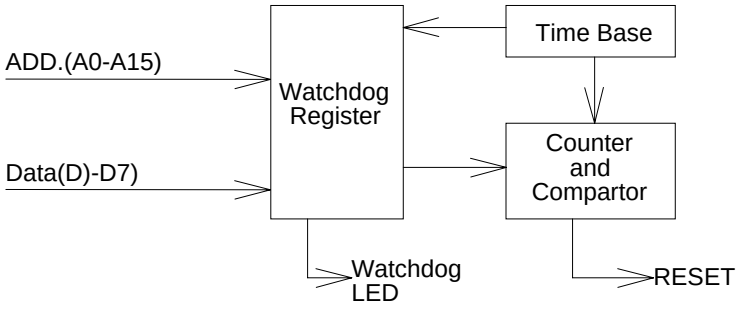
Step 2 Execute install.exe file.

Note: In the LAN directory, a HELPME.EXE file is included to provide installation information

Watchdog Timer

This section describes how to use the Watchdog Timer, including disabled, enabled, and trigger functions.

The FB2502 is equipped with a programmable time-out period watchdog timer. You can use your own program to enable the watchdog timer. Once you have enabled the watchdog timer, the program should trigger the I/O every time before the timer times out. If your program fails to trigger or disable this timer before it times out, e.g. because of a system hang-up, it will generate a reset signal to reset the system. The time-out period can be programmed to be set from 1 to 255 seconds or minutes.



The CD –ROM includes a Watch Dog demo file. In the file, there are 3 execution programs written in different forms. The sub-directories of the file are:

1. WATCHDOG/ASSEMBLE: Library and Test Program written in Assembly Language

2. WATCHDOG/TURBOC: Library and Test Program written in Turbo C++

The WATCHDOG includes a demonstration program established for users who would like to configure the Watchdog timer by themselves.

Note: In the WATCHDOG directory, README.TXT file is included to provide demo program information.

Watchdog Timer Setting

The watchdog timer is a circuit that may be used from your program software to detect system crashes or hang-ups. LED1 on this CPU board is the watchdog timer indicator, which is located at the upper-left corner above the USB connector. Whenever the watchdog timer is enabled, the LED will blink to indicate that the timer is counting. The watchdog timer is automatically disabled after reset.

Once you have enabled the watchdog timer, your program must trigger the watchdog timer every time before it times out. After you trigger the watchdog timer, it will be set to non-zero value to watchdog counter and start to count down again. If your program fails to trigger the watchdog timer before time-out, it will generate a reset pulse to reset the system.

The factor of the watchdog timer time-out constant is approximately 1 seconds. The period for the watchdog timer time-out is between 1 to FF timer factors.

If you want to reset your system when watchdog times out, the following table listed the relation of timer factors between time-out periods.

Time Factor	Time-Out Period (Seconds)	Time-Out Period (Minutes)
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
“	“	“
“	“	“
“	“	“
FF	FF	FF

Watchdog Timer Enabled

To enable the watchdog timer, you have to output a byte of timer factor to the watchdog. The following is a Turbo C++ program, which demonstrates how to enable the watchdog timer and set the time-out period at 6 seconds.

```
#include “stdio.H”
#include “WDLIB.H”

main( )
{
char WD_TIME=ox6;

InitWD(equWdUnitS);
printf (“Enable watchdog”);
//Trigger watchdog Timer Output is 6 seconds
EnWD(WD_TIME);
}
```

Watchdog Timer Trigger

After you enable the watchdog timer, your program must write the same factor as enabling to the watchdog register at least once every time-out period to its previous setting. You can change the time-out period by writing another timer factor to the watchdog register at any time, and you must trigger the watchdog before the new time-out period in the next trigger. Below is a Turbo C++ program, which demonstrates how to trigger the watchdog timer:

```
#include “stdio.H”
#include “WDLIB.H”

main( )
{
char WD_TIME=ox6;

InitWD(equWdUnitS);
printf (“Enable watchdog”);
//Trigger watchdog Timer Output is 6 seconds
EnWD(WD_TIME);
}
```

Watchdog Timer Disabled

To disable the watchdog timer, simply write a 00H to the watchdog register.

```
#include “stdio.H”
#include “WDLIB.H”

main( )
{
InitWD(equWdUnitS);
printf (“Disable Watch Dog”);
//Disable watch dog
DisWD(WD_TIME);
}
```

Programming RS-485

The majority communicative operation of the RS-485 is in the same of the RS-232. When the RS-485 precedes the transmission, which needs control the TXC signal, and the installing, steps are as follows:

Step 1: Enable TXC

Step 2: Send out data

Step 3: Waiting for data empty

Step 4: Disable TXC

Note: Please refer to the section of the “Serial Ports” in the Chapter “System Controllers” for the detail description of the COM port’s register.

❑ **Initialize COM port**

Step 1: Initialize COM port in the receiver interrupt mode, and /or transmitter interrupt mode. (All of the communication protocol buses of the RS-485 are in the same.)

Step 2: Disable TXC (transmitter control), the bit 0 of the address of offset+4 just sets "0".

NOTE: Control the FB2502 CPU card's DTR signal to the RS-485's TXC communication.

❑ **Send out one character (Transmit)**

Step 1: Enable TXC signal, and the bit 0 of the address of offset+4 just sets "1".

Step 2: Send out the data. (Write this character to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data empty. Check transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are all sets must be "0".

Step 4: Disabled TXC signal, and the bit 0 of the address of offset+4 sets "0"

❑ **Send out one block data (Transmit – the data more than two characters)**

Step 1: Enable TXC signal, and the bit 0 of the address of offset+4 just sets "1".

Step 2: Send out the data. (Write all data to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data empty. Check transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are all sets must be "0".

Step 4: Disabled TXC signal, and the bit 0 of the address of offset+4 sets "0"

- **Receive data**

The RS-485's operation of receiving data is in the same of the RS-232's.

- **Basic Language Example**

a. Initial 86C450 UART

```
10      OPEN "COM1:9600,m,8,1"AS #1 LEN=1
20      REM Reset DTR
30      OUT &H3FC, (INP(%H3FC) AND &HFA)
40      RETURN
```

b. Send out one character to COM1

```
10      REM Enable transmitter by setting DTR ON
20      OUT &H3FC, (INP(&H3FC) OR &H01)
30      REM Send out one character
40      PRINT #1, OUTCHR$
50      REM Check transmitter holding register and shift register
60      IF ((INP(&H3FD) AND &H60) >0) THEN 60
70      REM Disable transmitter by resetting DTR
80      OUT &H3FC, (INP(&H3FC) AND &HEF)
90      RETURN
```

- **c. Receive one character from COM1**

```
10      REM Check COM1: receiver buffer
20      IF LOF(1)<256 THEN 70
30      REM Receiver buffer is empty
40      INPSTR$"
```

```
50      RETURN

60      REM Read one character from COM1: buffer

70      INPSTR$=INPUT$(1,#1)

80      RETURN
```

NOTE: The example of the above program is based on COM1 (I/O Address 3F8h). The RS-485 of the FB2502 uses COM2. If you want to program it, please refer to the BIOS Setup for COM2 address setup.

Chapter 7 Technical Reference

This section outlines the errors that may occur when you operate the system, and also gives you the suggestions on solving the problems.

Topic include:

- Trouble Shooting for Error Messages
- Technical Reference

Trouble Shooting for Error Messages

The following information informs the error messages and troubleshooting. Please adjust your systems according to the messages below. Make sure all the components and connectors are in proper position and firmly attached. If the errors still exist, please contact with your distributor for maintenance.

- **POST BEEP**

Currently there are two kinds of beep codes in BIOS setup.

- One indicates that a video error has occurred and the BIOS cannot initialize the video screen to display any additional information. This beep code consists of a single long beep followed by three short beeps.
- The other indicates that an error has occurred in your DRAM. This beep code consists of a constant single long beep.

- **CMOS BATTERY FAILURE**

When the CMOS battery is out of work or has run out, the user has to replace it with a new battery.

- **CMOS CHECKSUM ERROR**

This error informs that the CMOS has corrupted. When the battery runs weak, this situation might happen. Please check the battery and change a new one when necessary.

- **DISPLAY SWITCH IS SET INCORRECTLY**

Display switch on the motherboard can be set to either monochrome or color. This indicates the switch is set to a different setting than indicated in BIOS Setup. Determine which setting is correct, and then either turn off the system and change the jumper, or enter BIOS Setup and change the video selection.

- **DISK BOOT FAILURE**

When you can't find the boot device, insert a system disk into Drive A and press < Enter >. Make sure both the controller and cables are all in proper positions, and also make sure the disk is formatted. Then reboot the system.

- **DISKETTE DRIVES OR TYPES MISMATCH ERROR**

When the diskette drive type is different from CMOS, please run setup or configure the drive again.

- **ERROR ENCOUNTERED INITIALIZING HARD DRIVE**

When you can't initialize the hard drive, ensure the following things:

1. The adapter is installed correctly
2. All cables are correctly and firmly attached
3. The correct hard drive type is selected in BIOS Setup

- **ERROR INITIALIZING HARD DISK CONTROLLER**

When this error occurs, ensure the following things:

1. The cord is exactly installed in the bus.
2. The correct hard drive type is selected in BIOS Setup
3. Whether all of the jumpers are set correctly in the hard drive

- **FLOPPY DISK CONTROLLER ERROR OR NO CONTROLLER PRESENT**

When you cannot find or initialize the floppy drive controller, please ensure the controller is in proper BIOS Setup. If there is no floppy drive installed, ensure the Diskette Drive selection in Setup is set to NONE.

- **KEYBOARD ERROR OR NO KEYBOARD PRESENT**

When this situation happens, please check keyboard attachment and no keys being pressed during the boot. If you are purposely configuring the system without a keyboard, set the error halt condition in BIOS Setup to HALT ON ALL, BUT KEYBOARD. This will cause the BIOS to ignore the missing keyboard and continue the boot procedure.

- **MEMORY ADDRESS ERROR**

When the memory address indicates error. You can use this location along with the memory map for your system to find and replace the bad memory chips.

- **MEMORY SIZE HAS CHANGED**

Memory has been added or removed since last boot. In EISA mode, use Configuration Utility to re-configure the memory configuration. In ISA mode enter BIOS Setup and enter the new memory size in the memory fields.

- **MEMORY VERIFYING ERROR**

It indicates an error verifying a value is already written to memory. Use the location along with your system's memory map to locate the bad chip.

- **OFFENDING ADDRESS MISSING**

This message is used in connection with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

- **REBOOT ERROR**

When this error occurs that requires you to reboot. Press any key and the system will reboot.

- **SYSTEM HALTED**

Indicates the present boot attempt has been aborted and the system must be rebooted. Press and hold down the CTRL and ALT keys and press DEL.

Technical Reference

Real-Time Clock and Non-Volatile RAM

The FB2502 contains a real-time clock compartment that maintains the date and time in addition to storing configuration information about the computer system. It contains 14 bytes of clock and control registers and 114 bytes of general purpose RAM. Because of the use of CMOS technology, it consumes very little power and can be maintained for long periods of time using an internal Lithium battery. The contents of each byte in the CMOS RAM are listed below:

Address	Description
00	Seconds
01	Second alarm
02	Minutes
03	Minute alarm
04	Hours
05	Hour alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status register A
0B	Status register B
0C	Status register C
0D	Status register D
0E	Diagnostic status byte
0F	Shutdown status byte
10	Diskette drive type byte, drive A and B
11	Fixed disk type byte, drive C
12	Fixed disk type byte, drive D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte

Address	Description
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte CMOS checksum
30	Low actual expansion memory byte
31	High actual expansion memory byte
32	Date century byte
33	Information flags (set during power on)
34-7F	Reserved for system BIOS

CMOS RAM Map

Register	Description
00h -10h	Standard AT-compatible RTC and Status and Status Register data definitions
11h – 13h	Varies
14h	Equipment Bits 7-6 Number of Floppy Drives 00 1 Drive 01 2 Drives Bits 5-4 Monitor Type 00 Not CGA or MDA 01 40x25 CGA 01 2 Drives 80x25 CGA Bits 3 Display Enabled 0 Disabled 1 Enabled Bit 2 Keyboard Enabled 00 Not CGA or MDA 01 40x25 CGA 01 2 Drives 80x25 CGA Bit 1 Math Coprocessor Installed 0 Absent 1 Present Bit 0 Floppy Drive Installed 0 Disabled 1 Enabled
15h	Base Memory (in 1KB increments), Low Byte
16h	Base Memory (in 1KB increments), High Byte
17h	IBM-compatible memory (in 1KB increments), Low Byte
18h	IBM-compatible memory (in 1KB increments), High Byte (max 15 MB)
19h-2Dh	Varies
2Eh	Standard CMOS RAM checksum, high byte
2Fh	Standard CMOS RAM checksum, low byte
30h	IBM-compatible Extended Memory, Low Byte (POST) in KB
31h	IBM-compatible Extended Memory, High Byte (POST) in KB
32h	Century Byte
33h	Reserved. Do not use
34h	Reserved. Do not use
35h	Low byte of extended memory (POST) in 64 KB
36h	High byte of extended memory (POST) in 64 KB
37h-3Dh	Varies
3Eh	Extended CMOS Checksum, Low Byte (including 34h-3Dh)
3Fh	Extended CMOS Checksum, High Byte (including 34h-3Dh)

I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses, which also becomes the identity of the device. There is a total of 1K-port address space available. The following table lists the I/O port addresses used on the Industrial CPU Card.

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 03Fh	Interrupt Controller #1
040h - 05Fh	Timer
060h - 06Fh	Keyboard Controller
070h - 07Fh	Real Time Clock, NMI
080h - 09Fh	DMA Page Register
0A0h - 0BFh	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #2
0F0h	Clear Math Coprocessor Busy Signal
0F1h	Reset Math Coprocessor
1F0h - 1F7h	IDE Interface
278 - 27F	Parallel Port #2(LPT2)
2F8h - 2FFh	Serial Port #2(COM2)
2B0 - 2DF	Graphics adapter Controller
378h - 3FFh	Parallel Port #1(LPT1)
360 - 36F	Network Ports
3B0 - 3BF	Monochrome & Printer adapter
3C0 - 3CF	EGA adapter
3D0 - 3DF	CGA adapter
3F0h - 3F7h	Floppy Disk Controller
3F8h - 3FFh	Serial Port #1(COM1)

Interrupt Request Lines (IRQ)

There are a total of 15 IRQ lines available on the Industrial CPU Card. Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on the Industrial CPU Card.

Level	Function
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ2	Interrupt Cascade
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ5	Parallel Port #2
IRQ6	Floppy Disk Controller
IRQ7	Parallel Port #1
IRQ8	Real Time Clock
IRQ9	Software Redirected to Int 0Ah
IRQ10	Reserved
IRQ11	Reserved
IRQ12	Reserved
IRQ13	Math coprocessor
IRQ14	Primary IDE
IRQ15	Secondary IDE

DMA Channel Map

The equivalent of two 8237A DMA controllers are implemented in the FB2650 board. Each controller is a four-channel DMA device that will generate the memory addresses and control signals necessary to transfer information directly between a peripheral device and memory. This allows high speeding information transfer with less CPU intervention. The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 channel 0 provides the cascade interconnection between the two DMA devices, thereby maintaining IBM PC/AT compatibility.

The following is the system information of DMA channels:

DMA Controller 1	DMA Controller 2
Channel 0: Spare	Channel 4: Cascade for controller 1
Channel 1: Reserved for IBM SDLC	Channel 5: Spare
Channel 2: Diskette adapter	Channel 6: Spare
Channel 3: Spare	Channel 7: Spare

Serial Ports

The ACEs (Asynchronous Communication Elements ACE1 to ACE2) are used to convert parallel data to a serial format on the transmit side and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five-bit format only) or two stop bits. The ACEs are capable of handling divisors of 1 to 65535, and produce a 16x clock for driving the internal transmitter logic.

Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the ACE a completed MODEM control capability, and a processor interrupt system that may be software tailored to the computing time required to handle the communications link.

The following table is a summary of each ACE accessible register

DLAB	Port Address	Register
0	Base + 0	Receiver buffer (read)
		Transmitter holding register (write)
0	Base + 1	Interrupt enable
X	Base + 2	Interrupt identification (read only)
X	Base + 3	Line control
X	Base + 4	MODEM control
X	Base + 5	Line status
X	Base + 6	MODEM status
X	Base + 7	Scratched register
1	Base + 0	Divisor latch (least significant byte)
1	Base + 1	Divisor latch (most significant byte)

- **Receiver Buffer Register (RBR)**

Bit 0-7: Received data byte (Read Only)

- **Transmitter Holding Register (THR)**

Bit 0-7: Transmitter holding data byte (Write Only)

- **Interrupt Enable Register (IER)**

Bit 0: Enable Received Data Available Interrupt (ERBFI)

Bit 1: Enable Transmitter Holding Empty Interrupt (ETBEI)

Bit 2: Enable Receiver Line Status Interrupt (ELSI)

Bit 3: Enable MODEM Status Interrupt (EDSSI)

Bit 4: Must be 0

Bit 5: Must be 0

Bit 6: Must be 0

Bit 7: Must be 0

- **Interrupt Identification Register (IIR)**

Bit 0: "0" if Interrupt Pending

Bit 1: Interrupt ID Bit 0

Bit 2: Interrupt ID Bit 1

Bit 3: Must be 0

Bit 4: Must be 0

Bit 5: Must be 0

Bit 6: Must be 0

Bit 7: Must be 0

- **Line Control Register (LCR)**

Bit 0: Word Length Select Bit 0 (WLS0)

Bit 1: Word Length Select Bit 1 (WLS1)

WLS1	WLS0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: Number of Stop Bit (STB)

Bit 3: Parity Enable (PEN)

Bit 4: Even Parity Select (EPS)

Bit 5: Stick Parity

Bit 6: Set Break

Bit 7: Divisor Latch Access Bit (DLAB)

- **MODEM Control Register (MCR)**

Bit 0: Data Terminal Ready (DTR)

Bit 1: Request to Send (RTS)

Bit 2: Out 1 (OUT 1)

Bit 3: Out 2 (OUT 2)

Bit 4: Loop

Bit 5: Must be 0

Bit 6: Must be 0

Bit 7: Must be 0

- **Line Status Register (LSR)**

Bit 0: Data Ready (DR)

Bit 1: Overrun Error (OR)

Bit 2: Parity Error (PE)

Bit 3: Framing Error (FE)

Bit 4: Break Interrupt (BI)

Bit 5: Transmitter Holding Register Empty (THRE)

Bit 6: Transmitter Shift Register Empty (TSRE)

Bit 7: Must be 0

- **MODEM Status Register (MSR)**

Bit 0: Delta Clear to Send (DCTS)

Bit 1: Delta Data Set Ready (DDSR)

Bit 2: Training Edge Ring Indicator (TERI)

Bit 3: Delta Receive Line Signal Detect (DSLSD)

Bit 4: Clear to Send (CTS)

Bit 5: Data Set Ready (DSR)

Bit 6: Ring Indicator (RI)

Bit 7: Received Line Signal Detect (RSLD)

- **Divisor Latch (LS, MS)**

	LS	MS
Bit 0:	Bit 0	Bit 8
Bit 1:	Bit 1	Bit 9
Bit 2:	Bit 2	Bit 10
Bit 3:	Bit 3	Bit 11
Bit 4:	Bit 4	Bit 12
Bit 5:	Bit 5	Bit 13
Bit 6:	Bit 6	Bit 14
Bit 7:	Bit 7	Bit 15

Desired Baud Rate	Divisor Used to Generate 16x Clock
300	384
600	192
1200	96
1800	64
2400	48
3600	32
4800	24
9600	12
14400	8
19200	6
28800	4
38400	3
57600	2
115200	1

Parallel Ports

- **Register Address**

Port Address	Read/Write	Register
Base + 0	Write	Output data
Base + 0	Read	Input data
Base + 1	Read	Printer status buffer
Base + 2	Write	Printer control latch

- **Printer Interface Logic**

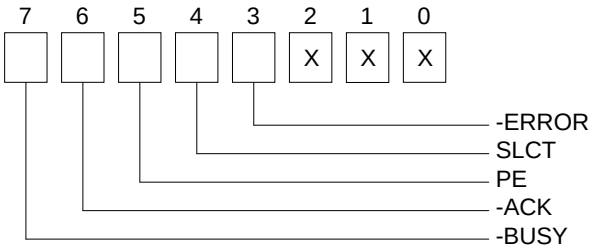
The parallel portion of the SMC37C669 makes the attachment of various devices that accept eight bits of parallel data at standard TTL level.

- **Data Swapper**

The system microprocessor can read the contents of the printer's Data Latch through the Data Swapper by reading the Data Swapper address

- **Printer Status Buffer**

The system microprocessor can read the printer status by reading the address of the Printer Status Buffer. The bit definitions are described below:



NOTE: X represents not used.

Bit 7: This signal may become active during data entry, when the printer is off-line during printing, or when the print head is changing position or in an error state. When Bit 7 is active, the printer is busy and cannot accept data.

Bit 6: This bit represents the current state of the printer's ACK signal. A 0 means the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before receiving a BUSY message stops.

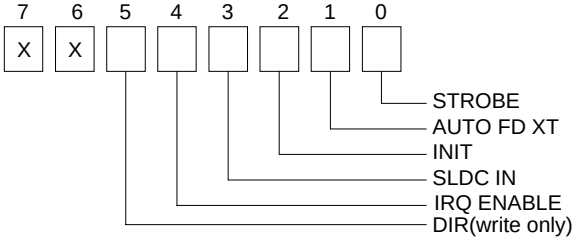
Bit 5: A 1 means the printer has detected the end of the paper.

Bit 4: A 1 means the printer is selected.

Bit 3: A 0 means the printer has encountered an error condition.

- **Printer Control Latch & Printer Control Swapper**

The system microprocessor can read the contents of the printer control latch by reading the address of printer control swapper. Bit definitions are as follows:



NOTE: X represents not used.

Bit 5: Direction control bit. When logic 1, the output buffers in the parallel port are disabled allowing data driven from external sources to be read, when logic 0 they work as a printer port. This bit is write-only.

Bit 4: A 1 in this position allows an interrupt to occur when ACK changes from low state to high state.

Bit 3: A 1 in this bit position selects the printer.

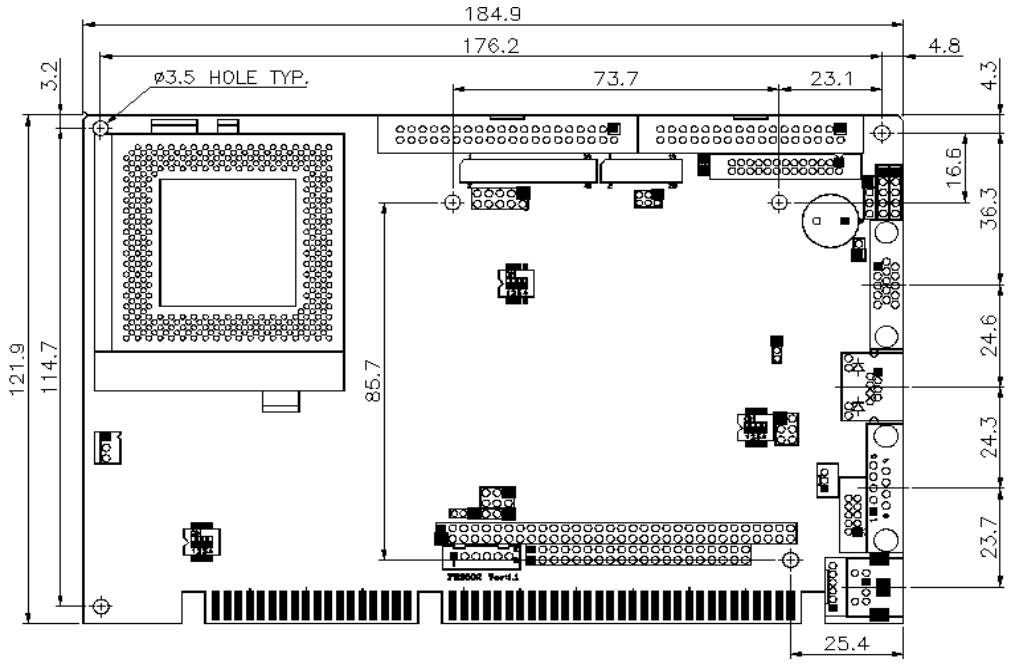
Bit 2: A 0 starts the printer (50 microseconds pulse, minimum).

Bit 1: A 1 causes the printer to line-feed after a line is printed.

Bit 0: A 0.5 microsecond minimum highly active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

Appendix

Dimension

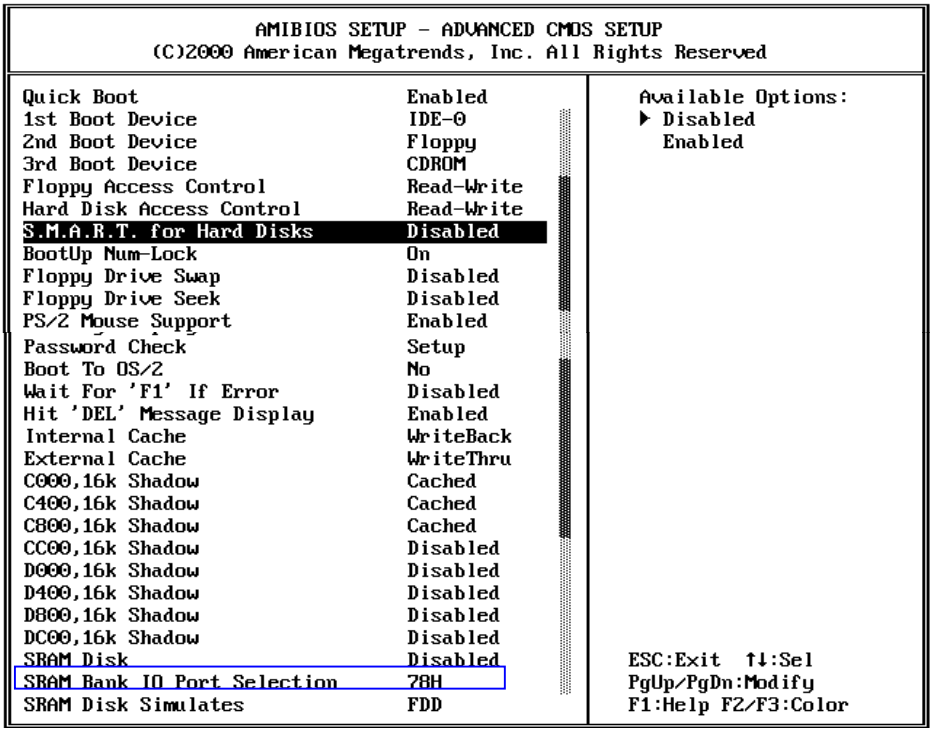


Unit: mm

SRAM memory banks

This provides the information about how to access the memory on the FB2502. The FB2502 hardware divides every 8K bytes of memory into a memory bank. To access the data in the memory, you have to assign a bank number. The memory bank number starts from zero. The last memory bank number depends on the size of the memory chip used on the FB2502. For example, if you use the 128K bytes memory chip, the bank number would be in the range of 0 to 15.

If a SRAM is installed to the system, the BIOS CMOS SETUP is determined by select 68h or 78h.



The I/O port address of the bank select base port 78h or 68h, the following is the format of the chip select and bank enable.

Register	I/O Port	D7	D6	D5	D4	D3	D2	D1	D0
Bank select	Base 0	Sel2	Sel1	A5	A4	A3	A2	A1	A0

SRAM	Sel2	Sel1
U14	0	1
U6	1	0
U24	1	1
Disable	0	0

Where:

Sel~Sel2 Select the SRAM CHIP's
A5~A0 Bank select bits, A0 is the LSB

For different types of memory, A0 to A5 have different explanations. These bits are used to select the bank number.

Memory	A5	A4	A3	A2	A1	A0
128KB SRAM	0	1	BS3	BS2	BS1	BS0
512KB SRAM	BS5	BS4	BS3	BS2	BS1	BS0

NOTE: BS0 to BS5 are the memory bank select bits. For example, 128KB memory has sixteen 8K-byte banks; so 4 bits (BS0 to BS3) are needed.

Example: Select the 10th bank of the U7 on the FB2502. Using CXK581000P/M (128K*8), and the base port is &H78.

```
100 base_port=&H78
110 OUT base_port,&H19
```

SRAM TYPE SUPPORTED

The following list contains SRAMs supported by the FB2502:

AKM	AKM628128	(128KX8, 1M bits)
HITACHI	HM628128	(128KX8, 1M bits)
NEC	UPD431000A	(128KX8, 1M bits)
SONY	CXK581000P/M	(128KX8, 1M bits)
HITACHI	HM628512	(512KX8, 4M bits)
NEC	UPD434000	(512KX8, 4M bits)
SONY	CXK584000P/M	(512KX8, 4M bits)